Agenda

• Electrical specifications
  – Noise margin
  – Fan-out
  – Static/Quiescent Power
  – Dynamic Power
  – Propagation Delay

• Configurations
  – Diode
  – Resistor pull-up (BJT and NMOS)
  – CMOS
  – Dynamic logic
  – Transmission gate
Logic Inverter

- Digital signals are one of two possible states (on, off)
- Actual analog voltages get interpreted as either logic “1” logic “0” or “undefined”
  - Accounts for noise

Output voltage ranges for the 7400 ALS TTL logic family.
Input and Output Voltage Ranges

- Logic circuits need to specify...
  - Worst case voltages produced at the output ($V_{OH}$, $V_{OL}$)
  - Minimum acceptable voltages on the input ($V_{IH}$, $V_{IL}$)
  - Need $V_{OH} > V_{IH}$ and $V_{IL} > V_{OL}$

Voltage ranges for the 7400 ALS TTL logic family operated from a +5-V supply.
Fan-Out

• Output can only drive a limited number of additional gates
  • Limited by the current that can be supplied at the output
  • A certain input current is also needed to ensure that switching time is reasonable

• Take the ratio
  • Minimum of $I_{OH}/I_{IH}$ or $I_{OL}/I_{IL}$
  • For MOS logic, input $I = 0$
    • $I_{out} = C_{IN} \frac{dv}{dt}$
    • $C_{IN}$ depends on fan-out
    • Want short $dv/dt$

The inverter has a fan-out of 3 (i.e., the inverter drives 3 inputs).
Static Power Dissipation: Simplified Inverter

• Power delivered when logic levels are constant
  • Non-zero when there’s a connection from power to ground
    • 0 when $\bar{A}$ is high
    • $V_{ss}^2 / R$ when $\bar{A}$ is low
    • Typically ranges from microwatts to milliwatts depending on logic family

• Power dissipation brings up issues involving
  • Temperature (heat sinks)
  • Battery lifetime
  • Power supply requirements
Dynamic Power Dissipation

- Power needed to charge up/down capacitors when there is a change in state
  - Typical capacitance: fF to pF range
- $P_{\text{dynamic}} = f \cdot C_{in} \cdot V_{ss}^2$
  - Energy stored in a capacitor: $\frac{1}{2} C_L V_{ss}^2$ (units: Joules)
  - All the stored energy in cap is dissipated in the switch in H to L transition (half-cycle)
- Power = Energy per unit time

Total Power Dissipation = $P_{\text{static}} + P_{\text{dynamic}}$

Load capacitance causes dynamic power dissipation in a logic gate.
Propagation Delay, Rise and Fall Time

- Due to capacitance, logic levels do not go from high to low instantly
- Rise/fall times: $t_r$, $t_f$
  - Time it takes to go between the 10% and 90% points
- Propagation delay: $t_{PHL}$, $t_{PLH}$
  - Time it takes for the output to transition, compared to the input
  - Measured from 50% point

$$t_{pd} = \frac{t_{PHL} + t_{PLH}}{2}$$
Propagation Delay can give rise to “Glitches”

A glitch in the output of the AND gate caused by propagation delay in the inverter.
Note that we have assumed zero delay for the AND gate.

To prevent glitching, clock the signals using a latch.
Diode Logic (Section 3.6)

- Limitations
  - Voltage drop of 0.7 v across each gate (cascading problems)
  - Can’t implement an inverter

Figure 3.23  Diode logic gates.
BJT Digital Logic (Section 4.9)

- Early on, the BJT was used as logic switch in a logic family known as resistor-transistor logic (RTL)
- RTL inverter
  - If input = 0, BJT operates in cutoff. No current passes through $R_c$ and $V_o$ equal to supply voltage
Load-Line Analysis

• For $V_{in} > 0.7$ v, the BJT turns on
  – Use input load-line to find base current
• Use a load-line on the output characteristics to find $V_o$
  – Minimum $V_{OL} = 0.2$ v

\[
V_{in} - R_B i_b - V_{BE} = 0
\]
\[
i_b = -\frac{1}{R_B} V_{BE} + \frac{V_{in}}{R_B}
\]

\[
V_{cc} - R_c i_c - V_{CE} = 0
\]
\[
i_c = -\frac{1}{R_c} V_{CE} + \frac{V_{cc}}{R_c}
\]

Note: assumes no loading
Transfer Characteristics

- Switching depends on $\beta$, $R_c$, and $R_b$
  - See Figure 4.44, Exercise 4.27
- $V_{OH}$ drops below $V_{CC}$ after loading the circuit
  - Similar cascading issues as diode logic
RTL NOR Gate

• If anyone of the inputs is high, then the corresponding BJT will conduct, pulling the output node down

• NOR gates can be used to generate any other digital logic gate (see Figure 6.6)
**NMOS Inverter with Pull-Up Resistor**

- Similar to BJT RTL inverter
- If $V_I = \text{low}$, transistor is in cutoff ($V_O = V_{DD}$)
- If $V_I = \text{high}$, transistor is in linear mode ($V_O = V_{DS} = \text{low}$)
  - Model transistor as a resistor and use voltage division

\[
I_d = KP \frac{W}{L} \left[ (V_{GS} - V_{to})V_{DS} - \frac{V_{DS}^2}{2} \right] \\
(V_{DS} << V_{GS} - V_{to})
\]

\[
I_d = KP \frac{W}{L} (V_{GS} - V_{to})V_{DS}
\]

\[
R_{on} = \frac{V_{DS}}{I_d} = \frac{1}{KP \frac{W}{L} (V_{GS} - V_{to})}
\]

Use large W/L ratio to keep $R_{on}$ small

$V_{OH} = V_{DD}$
$V_{OL} = \frac{R_{on}}{R_{D} + R_{on}} V_{DD}$

Want $R_{on} \ll R_D$ for good noise margin ($V_{OL} \sim 0$)

90 kΩ
Loadline Analysis for the NMOS Inverter

\[ V_{DD} - i_D R_D + V_{DS} = 0 \]

\[ i_D = -\frac{1}{R_D} V_{DS} + \frac{V_{DD}}{R_D} \]

\[ V_I = V_{GS} = V_{DD} = 5 \text{ V} \]

\[ V_I = V_{GS} = 0 \text{ V} \]

\[ V_O = V_{DS} = 5 \text{ V} \]

\[ V_{TO} = 1 \text{ V} \]

\[ K_P = 50 \mu A/V^2 \]

\[ \lambda = 0 \]

\[ W/L = 1/2 \]
Inverter Transfer Characteristic

- Define $V_{IL}$ and $V_{IH}$ as points where the slope $= -1$
Low to High Output Transition

- $V_I = V_{DD}$ to 0
  - NMOS turns off
- $V_o = \text{low (} V_{OH} \text{)}$ to $V_{DD}$
  - Transient response resembles an RC circuit
    - Time constant = $R_D C$

![Diagram of low to high output transition with NMOS and RC circuit components.]
Loadline Analysis of the High-to-Low Transition

- $V_I = 0$ to $V_{DD}$
  - NMOS turns on (saturation, then linear)
  - $V_o = V_{DD}$ to low
- Travels in a path from A to B to C
  - Load capacitor cannot instantaneously change voltage
- Maximum current during discharge = 200 $\mu$A

Maximum current during L-to-H transition:
$5 \text{ V} / 90 \text{ k$\Omega$} = 55 \mu$A (results in $t_{PHL} < t_{PLH}$)
NMOS Transistor Pull-Up Inverter

- Eliminates area penalty due to $R_D$
  - 90 $k\Omega$ requires a $W = \text{min}$, $L = 360 \times \text{min layout}$
    - Assuming $R_{\text{sheet}} = 250 \ \Omega$/•
  - Pull-up transistor: $W = \text{min}$, $L = 3 \times \text{min layout}$
    - Small $W/L$ so that $R_D$ is large and $V_{OL}$ is low
    - Tradeoff: poor low to high transition (lower current during pull-up)

- Other disadvantages
  - $V_{OH}$ not $V_{DD}$ (due to $V_{TO}$ drop across transistor)
    - Worsened by $\gamma$ effect ($V_{TO}$ shift due to source/body voltage)

EE 171
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Other Pull-Up Configurations

• Use a higher gate voltage on the pull-up transistor
  • Eliminates $V_{OH}$ drop due to $V_{TO}$
  • Problem: requires 2 power supply voltages

• Use a depletion mode transistor as the pull-up
  • $V_{TO} < 0$
CMOS Inverter

- Load: PMOS transistor
  - $W/L$ 2x versus NMOS (IV characteristics are symmetrical)
  - No $V_{OH}$ drop due to $V_{TO}$
- No static power dissipation in either DC state
  - $V_I = \text{low}$: PMOS on, NMOS off
  - $V_I = \text{high}$: PMOS off, NMOS on
  - No resistive path from $V_{DD}$ to gnd
Graphical Analysis of a CMOS Inverter

Transfer Characteristics

A: NMOS cutoff, PMOS off
B: NMOS sat, PMOS linear
C: NMOS sat, PMOS sat
D: NMOS sat, PMOS sat
E: NMOS: linear, PMOS sat
F: NMOS: off, PMOS cutoff

\[ V_{GSP} = V_{GSN} - V_{DD} = V_1 - V_{DD} \]

\[ V_{DSN} = V_{DSP} + V_{DD} \]
Propagation Delay: High to Low Transition

- Current used to discharge the capacitor is NMOS saturation
  - Assume $\lambda = 0$ and $V_{DD}/2$ point is still in saturation
  - Similar equation for $t_{PLH}$ (use PMOS)

\[
t_{PHL} = \frac{Q}{I} = \frac{C_L \Delta V}{WKP} = \frac{V_{DD}}{2} (V_{GS} - V_{TO})^2 = \left(\frac{W}{L}\right)_N \frac{KP_N}{2} (V_{DD} - V_{TO})^2 = \left(\frac{W}{L}\right)_N KP_N (V_{DD} - V_{TO})^2
\]

A: initial condition ($V_{in} = \text{low, } V_{out} = \text{high}$)
B: $V_{in} = \text{high (capacitive load)}$
C: $V_{out} = 50\% \text{ point}$
CMOS Logic Gates

- 2-input NOR gate
  - If A or B is high, output is low
  - Output = high only if A and B are both low
- To maintain symmetry (transfer characteristic changes at $V_{DD}/2$), different W/L ratios may be used
  - 2-input NOR: $(W/L)_p = 4(W/L)_n$
  - 2-input NAND: $(W/L)_p = (W/L)_n$

Goal: effective PMOS W/L = 2x effective NMOS W/L
Two Input NAND Gate

Transfer Function

Results depend on which Inputs are switching
Dynamic Logic: NOR Gate

- Used to reduce transistor count
  - Use only NMOS transistors for logic operation
- Use an additional PMOS and NMOS device for clocking
  - If clock ($\phi$) = 0, output = high
  - If $\phi$ = high, output depends on NMOS transistors
    - Goes low if any of the A through M signals are high

Any other logic function can be generated from NOR gates.
CMOS Analog Switch (Pass Gate)

- Connects 1 to 2 if C is high
  - Use 2 transistors to avoid $V_{TO}$ drop
- Can be used to implement logic
- Can be used as a switch

(a) Equivalent circuit in which the switch is closed if C is high and open and if C is low (the on resistance $R_{on}$ is nonlinear)

(b) Circuit symbol

(a) NAND gate

(b) NOR gate

Network of switches