EE 171

Integrated Circuit Design
(Current Sources)

University of California, Santa Cruz
May 10, 2007
Agenda / Outline

• A discrete, multi-stage amplifier
  – (p. 343-348)

• Discrete versus IC design (Section 7.1)

• IC biasing using current sources
  – BJT implementations (Section 7.2)
  – MOS implementations (Section 7.3)
A Discrete Multi-Stage Amplifier

- Specs: p. 343
- Use emitter followers for high input and low output impedance
- Cascade two common-emitter amplifiers to get the desired gain
- Input impedance of each stage is important
  - $Z_{in}$ of emitter follower (last stage) = Load of emitter follower (3rd stage)
  - Will be used to determine the emitter resistances of the common-emitter stages

![Amplifier block diagram](image)
Circuit Implementation

Emitter Follower (1st stage)
- Need resistances above 1 MΩ to meet input impedance requirements
- Choose $R_3$ so that base current is lower than current through $R_1$ and $R_2$

Emitter Follower (last stage)
- Bias point chosen to avoid clipping
  - $V_{CE}$ (Q4): sufficient voltage swing
  - $I_C$ (Q4): sufficient current through $R_L$
Reduction of Discrete Elements

- Several coupling capacitors and resistors can be eliminated
  - DC operating point at the output can be used as the input of the next stage
  - Still need coupling between 2\textsuperscript{nd} and 3\textsuperscript{rd} stage (want $V_{CE} = 5$ v and in the middle of the 15 v supply)
Final Implementation

- Resistors chosen so that collector currents go from \( \mu A \) to mA
  - Gradual change from high impedance to low impedance
- Capacitors: impedance should be low at high end of frequency range
  - Impedance should also be smaller than other nearby resistances at the low end of the frequency range (to avoid roll-off in gain)
What differs in IC biasing?

• Why integrated circuits?
  – Better density
  – Better matching from one device to the next

• In discrete applications, use resistors and capacitors for biasing
  – Very large range of values

• However in IC applications, it is expensive to use these devices
  – Occupies a lot of chip area
  – 1 µF capacitor: 12,000 µm x 12,000 µm
  – 100 kΩ resistor: W = minimum rule, L = 400x longer

• For this reason, replace resistors with transistor where possible
  – Stages will also need to be directly coupled
IC Circuits: BJT or MOS?

- Circuit implementations shown can be done with BJTs or MOS transistors
  - Which is better?

- Using BJTs
  - Advantages
    - Higher current drive
    - Better switching characteristics
    - Able to support high power designs
  - Disadvantages
    - Always leaks
    - Not scalable ($V_{BE} = 0.7 \text{ v}$)

- Using MOS transistors
  - Smaller area (used for high density circuits)
  - Scalable
  - Easier to make (less process complexity vs. BJTs)
  - 0 static power dissipation (input is an insulator)
Current Mirror

• Bias both Q₁ and Q₂ into active mode
  – By symmetry, $V_{BE1} = V_{BE2} = 0.7 \text{ v}$, and $I_{C1} = I_{C2}$

• KCL: $I_{\text{ref}} = I_{C1} + I_{B1} + I_{B2} \approx I_{C1}$ (low base currents)

• Junction areas can be scaled without affecting symmetry
  – Allows for $I_{C2} = a$ multiple of $I_{\text{ref}}$

$$I_{\text{ref}} = \frac{V_{CC} - V_{BE1}}{R}$$

Output resistance

(Operate current mirror in this area)

IV looks like a single BJT curve
Application: Biasing an Emitter Follower

- Eliminates two resistors
- Note that input and output are directly coupled
  - Output will have a DC offset of $-0.7\,\text{v}$ ($V_{BE}$ of $Q_3$)
  - Can eliminate this by cascading with a PNP follower
Widlar Current Source

- $I_{C1}$ semi-arbitrary (used to choose $R_1$)
- Choose $R_2$ based on requirements of $I_{C2}$ (current source)
  - KVL: $V_{BE1} - V_{BE2} - R_2 I_{C2} = 0$
- Can be used to design current sources with lower resistances
  - See Example 7.3

\[
I_E = I_B + I_C = I_{ES} \left( e^{\frac{V_{BE}}{V_T}} - 1 \right)
\]

\[
I_C \approx I_{ES} e^{\frac{V_{BE}}{V_T}}
\]

\[
V_{BE} = V_T \ln \frac{I_C}{I_{ES}}
\]

\[
I_{C1} \approx \frac{V_{CC} - V_{BE1}}{R_1}
\]

\[
R_2 \approx \frac{V_T}{I_{C2}} \ln \frac{I_{C1}}{I_{C2}}
\]
Multiple Current Sources

• In a typical IC biasing, the same reference current can be used for several current sources
  – See Exercise 7.3

• Current source
  – NPN circuit
  – Removes current from the circuit

• Current sink
  – PNP circuit
  – Delivers current to the circuit

\[ I_{\text{ref}} = \frac{(15 - 0.7) - (-15 + 0.7)}{R_1} \]
Biasing with FETs (Current Mirror)

- The same biasing configurations can be applied to MOS transistors
- $M_1$ is in saturation
  - $V_{DS1} = V_{GS1}$
  - Saturation: $V_{DS} > V_{GS} - V_T$
  - By symmetry, $I_o = I_1$
    - Independent of $V_o$ (as long as $M_2$ is biased into saturation)
- For a different $I_o$ value, the W/L ratios of the transistors can be changed

\[
I_o = \frac{W_2}{L_2} \frac{W_1}{L_1} I_1
\]

\[
R_{out} = r_d
\]
NMOS Wilson current source

- Higher output resistance
  - Proof: draw the small signal AC circuit and find $Z_{\text{out}}$

\[ I_1 = \frac{V_{DD} - 2V_{t_0}}{R} \]