P10.34 An ideal diode acts as a short circuit as long as current flows in the forward direction. It acts as an open circuit provided that there is reverse voltage across it. The volt-ampere characteristic is shown in Figure 10.15 in the text. After solving a circuit with ideal diodes, we must check to see that forward current flows in diodes assumed to be on, and we must check to see that reverse voltage appears across all diodes assumed to be off.

P10.35 The equivalent circuit for two ideal diodes in series pointing in opposite directions is an open circuit because current cannot flow in the reverse direction for either diode.

The equivalent circuit for two ideal diodes in parallel pointing in opposite directions is a short circuit because one of the diodes is forward conducting for either direction of current flow.

P10.36 (a) The diode is on, $V = 0$ and $I = \frac{10}{2700} = 3.70$ mA.

(b) The diode is off, $I = 0$ and $V = 10$ V.

(c) The diode is on, $V = 0$ and $I = 0$.

(d) The diode is on, $I = 5$ mA and $V = 5$ V.
P10.62  A clipper circuit removes or clips part of the input waveform. An example circuit with waveforms is:

![Clipper Circuit Diagram]

We have assumed a forward drop of 0.6V for the diode.

P10.63  Refer to Figure P10.63 in the book. When the source voltage is negative, diode $D_3$ is on and the output $\nu_o(t)$ is zero. For source voltages between 0 and 10 V, none of the diodes conducts and $\nu_o(t) = \nu_s(t)$. Finally when the source voltage exceeds 10 V, $D_1$ is on and $D_2$ is in the breakdown region so the output voltage is 10 V. The waveform is:

![Waveform Diagram]
(a) A suitable circuit is:

![Circuit Diagram](image)

We choose the resistors $R_1$ and $R_2$ to achieve the desired slope.

$$\text{Slope} = \frac{1}{3} = \frac{R_2}{R_1 + R_2}$$

Thus, choose $R_1 = 2R_2$. For example, $R_1 = 2 \, \text{k}\Omega$ and $R_2 = 1 \, \text{k}\Omega$.

(b) A suitable circuit is:

![Circuit Diagram](image)

Other resistor values will work, but we must make sure that $D_2$ remains forward biased for all values of $v_m$, including $v_m = -10 \, \text{V}$. To achieve the desired slope (i.e., the slope is 0.5) for the transfer characteristic, we must have $R_1 = R_2$. 

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P12.3* \[ K = \frac{1}{2} K(P_\text{W} / L) = 0.25 \text{mA/V}^2 \]

(a) Saturation because we have \( v_{\text{GS}} \geq V_{\text{to}} \) and \( v_{\text{DS}} \geq v_{\text{GS}} - V_{\text{to}} \).

\[ i_D = K(v_{\text{GS}} - V_{\text{to}})^2 = 2.25 \text{mA} \]

(b) Triode because we have \( v_{\text{DS}} < v_{\text{GS}} - V_{\text{to}} \) and \( v_{\text{GS}} \geq V_{\text{to}} \).

\[ i_D = K[2(v_{\text{GS}} - V_{\text{to}})v_{\text{DS}} - v_{\text{DS}}^2] = 2 \text{mA} \]

(c) Cutoff because we have \( v_{\text{GS}} \leq V_{\text{to}} \). \( i_D = 0 \).

P12.4* \[ i_D \]

P12.5 The device is in saturation for \( v_{\text{DS}} \geq v_{\text{GS}} - V_{\text{to}} = 3 \text{V} \). The device is in the triode region for \( v_{\text{DS}} \leq 3 \text{V} \). In the saturation region, we have

\[ i_D = K(v_{\text{GS}} - V_{\text{to}})^2 = 0.1(v_{\text{GS}} - 1)^2 \text{ for } v_{\text{GS}} \geq 1 \]

In the pinchoff region, we have

\[ i_D = 0 \text{ for } v_{\text{GS}} \leq 1 \]

The plot of \( i_D \) versus \( v_{\text{GS}} \) in the saturation region is:
(a) Saturation because we have $v_{GS} \geq V_{to}$ and $v_{DS} \geq v_{GS} - V_{to}$.
(b) Triode because we have $v_{GS} \geq V_{to}$ and $v_{DS} \leq v_{GS} - V_{to}$.
(c) Saturation because we have $v_{GS} \geq V_{to}$ and $v_{DS} \geq v_{GS} - V_{to}$.
(d) Cutoff because we have $v_{GS} \leq V_{to}$.

With the gate connected to the drain, we have $v_{DS} = v_{GS}$ so $v_{DS} \geq v_{GS} - V_{to}$. Then, if $v_{GS}$ is greater than the threshold voltage, the device is operating in the saturation region. If $v_{GS}$ is less than the threshold voltage, the device is operating in the cutoff region.

For the NMOS enhancement transistors, we have $V_{to} = +1$ V. For the PMOS enhancement transistors, we have $V_{to} = -1$ V.

(a) This NMOS transistor is operating in saturation because we have $v_{GS} \geq V_{to}$ and $v_{DS} \geq v_{GS} - V_{to}$. Thus, $I_a = k(v_{GS} - V_{to})^2 = 0.9$ mA.
(b) This PMOS transistor is operating in saturation because we have $v_{GS} \leq V_{to}$ and $v_{DS} = -4 \leq v_{GS} - V_{to} = -3 -(-1) = -2$. Thus, $I_b = k(v_{GS} - V_{to})^2 = 0.4$ mA.
(c) This PMOS transistor is operating in the triode region because we have $v_{GS} \leq V_{to}$ and $v_{DS} = -1 \geq v_{GS} - V_{to} = -5 -(-1) = -4$. Thus, $I_c = k[2(v_{GS} - V_{to})v_{DS} - v_{DS}^2] = 0.7$ mA.
(d) This NMOS transistor is operating in the triode region because we have $v_{GS} \geq V_{to}$ and $v_{DS} = 1 \leq v_{GS} - V_{to} = 3 - 2 = 1$. Thus, $I_d = k[2(v_{GS} - V_{to})v_{DS} - v_{DS}^2] = 0.3$ mA.

With $v_{GS} = v_{DS} = 5$ V, the transistor operates in the saturation region for which we have $i_D = k(v_{GS} - V_{to})^2$. Solving for $k$ and substituting values we obtain $k = 125 \mu A/V^2$. However we have $k = (W/L)(KP/2)$. Solving for $W/L$ and substituting values we obtain $W/L = 5$. Thus for $L = 2 \mu m$, we need $W = 10 \mu m$.

To obtain the least drain current choose minimum $W$ and maximum $L$ (i.e., $W_1 = 0.25 \mu m$ and $L_1 = 2 \mu m$). To obtain the greatest drain current choose maximum $W$ and minimum $L$ (i.e., $W_2 = 2 \mu m$ and $L_2 = 0.25 \mu m$). The ratio between the greatest and least drain current is $(W_2/L_2)/(W_1/L_1) = 64$.

In the saturation region, we have $i_D = k(v_{GS} - V_{to})^2$. Substituting values, we obtain two equations:
With $V_{in} = 0$, the transistor operates in saturation and $I_b = I_D = K(v_{GS} - V_{to})^2 = 3.2 \text{ mA}$. With $V_{in} = 5$, the transistor operates in cutoff and $I_b = i_D = 0$.

**P12.14** Because $v_{GD} = 3 - 5 = -2 \text{ V}$ is less than $V_{to}$, the transistor is operating in saturation. Thus, we have $i_D = K(v_{GS} - V_{to})^2$. Substituting values gives $0.5 = 0.5(v_{GS} - 1)^2$ which yields two roots: $v_{GS} = 2$ and $v_{GS} = 0 \text{ V}$. However, the second root is extraneous, so we have $v_{GS} = 2 = 3 - 0.0005R$ which yields $R = 2000 \Omega$.

**P12.15** We have $i_D = K(v_{GS} - V_{to})^2$. Substituting values and solving, we obtain $v_{gs} = -2.5$ and $v_{gs} = 1.5 \text{ V}$. However, if $v_{gs} = 1.5$, the PMOS transistor is operating in cutoff. Thus, the correct answer is $v_{gs} = -2.5 \text{ V}$.

**P12.16** Distortion occurs in FET amplifiers because of curvature and nonuniform spacing of the characteristic curves.

**P12.17** The load-line equation is $V_{DD} = R_{D}i_D + v_{DS}$, and the plots are:

![Diagram](image)

Notice that the load line rotates around the point $(V_{DD}, 0)$ as the resistance changes.

**P12.18** The load-line equation is $V_{DD} = R_Di_D + v_{DS}$, and the plots are:
Notice that the load lines are parallel as long as $R_D$ is constant.

**P12.19** For $V_{GS} = 0$, the FET remains in cutoff so $V_{DS_{max}} = V_{DSQ} = V_{DS_{min}} = 20$ V. Thus, the output signal is zero, and the gain is zero. For amplification to take place, the FET must be biased in the saturation or triode regions.

**P12.20** (a) The 1.7 MΩ and 300 kΩ resistors act as a voltage divider that establishes a dc voltage $V_{GSQ} = 3$ V. Then if the capacitor is treated as a short for the ac signal, we have $v_{GS}(t) = 3 + \sin(2000\pi t)$ (b), (c), and (d)

From the load line we find $V_{DSQ} = 16$ V, $V_{DS_{max}} = 19$ V, and $V_{DS_{min}} = 11$ V.

**P12.21** For $v_{in} = +1$ V we have $V_{GS} = 4$ V. For the FET to remain in saturation, we
Notice that the load lines are parallel as long as $R_D$ is constant.

**P12.19** For $V_{GS} = 0$, the FET remains in cutoff so $V_{DS_{max}} = V_{DS_{Q}} = V_{DS_{min}} = 20$ V. Thus, the output signal is zero, and the gain is zero. For amplification to take place, the FET must be biased in the saturation or triode regions.

**P12.20** (a) The 1.7 MΩ and 300 kΩ resistors act as a voltage divider that establishes a dc voltage $V_{GS_{Q}} = 3$ V. Then if the capacitor is treated as a short for the ac signal, we have $v_{GS}(t) = 3 + \sin(2000\pi t)$ (b), (c), and (d)

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**P12.21** For $v_{in} = +1$ V we have $V_{GS} = 4$ V. For the FET to remain in saturation, we
P12.29* We can write $V_{dd} = 20 = 2I_{DQ} + 8 + 2$ in which $I_{DQ}$ is in mA. Solving, we obtain $I_{DQ} = 5$ mA. Then, we find $R_s = 2 / I_{DQ} = 400\Omega$. Next, we have $K = \frac{1}{2} KP(W \div L) = 0.75\ mA/V^2$. Assuming that the NMOS operates in saturation, we have

$$I_{DQ} = K(V_{GSQ} - V_t)^2$$

Substituting values and solving we find $V_{GSQ} = -1.582$ V and $V_{GSQ} = 3.582$ V. The correct root is $V_{GSQ} = 3.582$ V. (As a check, we see that the device does operate in saturation because we have $V_{DSQ} = 8$ V, which is greater than $V_{GSQ} - V_t$.) Then, we have $V_g = V_{GSQ} + 2 = 5.582$ V. However, we also have

$$V_g = V_{dd} \frac{R_2}{R_1 + R_2}$$

Substituting values and solving, we obtain $R_1 = 2.583 M\Omega$.

P12.30 First, we use Equation 12.11 to compute

$$V_g = V_{dd} \frac{R_2}{R_1 + R_2} = 5\ V$$

As in Example 12.2, we need to solve:

$$V_{GSQ}^2 + \left( \frac{1}{R_s K} - 2V_t \right) V_{GSQ} + (V_t)^2 - \frac{V_g}{R_s K} = 0$$

Substituting values, we have

$$V_{GSQ}^2 - 1.1489 V_{GSQ} - 3.2553 = 0$$

The roots are $V_{GSQ} = 2.4679$ V and $-1.319$ V. The correct root is $V_{GSQ} = 2.4679$ V which yields $I_{DQ} = K(V_{GSQ} - V_t)^2 = 0.5387$ mA. Finally, we have $V_{DSQ} = V_{dd} - R_0 I_{DQ} - R_3 I_{DQ} = 9.936$ V.

P12.31 Assuming that the MOSFET is in saturation, we have

$$V_{GSQ} = 10 - I_{DQ}$$

$$I_{DQ} = K(V_{GSQ} - V_t)^2$$
where we have assumed that $I_{DQ}$ and $K$ are in mA and mA/V^2 respectively.

(a) Using the second equation to substitute in the first, substituting values and rearranging, we have

$$V_{GSQ}^2 - 7V_{GSQ} + 6 = 0$$

which yields $V_{GSQ} = 6$ V. (The other root, $V_{GSQ} = 1$ V, is extraneous.)

$$I_{DQ} = 4 \text{ mA}$$

$$V_{DSQ} = 20 - 2I_{DQ} = 12 \text{ V}$$

(b) Similarly for the second set of values, we have

$$V_{GSQ}^2 - 3.5V_{GSQ} - 1 = 0$$

$$V_{GSQ} = 3.765 \text{ V}$$

$$I_{DQ} = 6.234 \text{ mA}$$

$$V_{DSQ} = 20 - 2I_{DQ} = 7.53 \text{ V}$$

P12.32 We can write $V_{dd} = R_1I_{DQ} + V_{DSQ} + R_sI_{DQ}$. Substituting values and solving we obtain $R_s = 3 \text{ k}\Omega$. Next we have $K = \frac{1}{2}KP(W/L) = 0.2 \text{ mA/V}^2$. Assuming that the NMOS operates in saturation, we have

$$I_{DQ} = K(V_{GSQ} - V_{th})^2$$

Substituting values and solving we find $V_{GSQ} = -1.236$ V and $V_{GSQ} = 3.236$ V. The correct root is $V_{GSQ} = 3.236$ V. (As a check we see that the device does operate in saturation because we have $V_{DSQ}$ greater than $V_{GSQ} - V_{th}$.) Then we have $V_G = V_{GSQ} + R_sI_{DQ} = 6.236 \text{ V}$. However we also have

$$V_G = V_{dd} \frac{R_2}{R_1 + R_2}$$

Substituting values and solving, we obtain $R_e = 1.082 \text{ M}\Omega$.

P12.33 We have $V_G = V_{GSQ} = 10R_2/(R_1 + R_2) = 2.5$ V. Then we have $I_{DQ} = K(V_{GSQ} - V_{th})^2 = 0.5625 \text{ mA}$. $V_{DSQ} = V_{dd} - R_0I_{DQ} = 4.375$ V.