Summary

1. If a differential amplifier has input voltages \(v_1\) and \(v_2\), the common-mode input is \(v_{\text{cm}} = \frac{1}{2}(v_1 + v_2)\) and the differential input signal is \(v_{\text{id}} = v_1 - v_2\).

2. An ideal operational amplifier has infinite input impedance, infinite gain for the differential input signal, zero gain for the common-mode input signal, zero output impedance, and infinite bandwidth.

3. In an amplifier circuit with negative feedback, part of the output is returned to the input. The feedback signal opposes the input source.

4. To analyze ideal op-amp circuits with negative feedback, we assume that the differential input voltage and the input current of the op amp are driven to zero (this is the summing-point constraint), and then we use basic circuit principles to analyze the circuit.

5. The basic inverting amplifier configuration is shown in Figure 14.4 on page 610. Its closed-loop voltage gain is \(A_V = -R_2/R_1\).

6. The basic noninverting amplifier configuration is shown in Figure 14.11 on page 618. Its closed-loop voltage gain is \(A_V = 1 + R_2/R_1\).

7. Many useful amplifier circuits can be designed using op amps. First, we select a suitable circuit configuration, and then we determine the resistor values that achieve the desired gain values.

8. In the design of op-amp circuits, very large resistances are unsuitable because their values are unstable and because high-impedance circuits are vulnerable to capacitive coupling of noise. Very low resistances are unsuitable because large currents flow in them for the voltages typically encountered in op-amp circuits.

9. In the linear range of operation, the imperfections of real op amps include finite input impedance, nonzero output impedance, and finite open-loop gain magnitude, which falls off with increasing frequency.

10. Negative feedback reduces gain magnitude and extends bandwidth. For the noninverting amplifier, the product of dc gain magnitude and bandwidth is constant for a given op-amp type.

11. The output voltage range and the output current range of any op amp are limited. If the output waveform reaches (and tries to exceed) either of these limits, clipping occurs.
12. The rate of change of the output voltage of any op amp is limited in magnitude. This is called the slew-rate limitation. The full-power bandwidth is the highest frequency for which the op amp can produce a full-amplitude sinusoidal output signal.

13. Dc imperfections of op amps are bias current, offset current, and offset voltage. These effects can be modeled by the sources shown in Figure 14.29 on page 636. The effect of dc imperfections is a (usually undesirable) dc component added to the intended output signal.

14. A single op amp can be used as a differential amplifier as shown in Figure 14.33 on page 640. However, the instrumentation amplifier shown in Figure 14.34 on page 641 has better performance.

15. The integrator circuit shown in Figure 14.35 on page 643 produces an output voltage that is proportional to the running-time integral of the input voltage. A differentiator circuit is shown in Figure 14.38 on page 645.

16. Active filters often have better performance than passive filters. Active Butterworth lowpass filters can be obtained by cascading several Sallen–Key circuits having the proper gains.

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**Problems**

**Section 14.1: Ideal Operational Amplifiers**

P14.1. A differential amplifier has input voltages \( v_1 \) and \( v_2 \). Give the definitions of the differential input voltage and of the common-mode input voltage.

P14.2. List the characteristics of an ideal op amp.

*P14.3. The input voltages of a differential amplifier are

\[
\begin{align*}
v_1(t) &= 0.5 \cos(2000\pi t) + 20 \cos(120\pi t) \\
v_2(t) &= -0.5 \cos(2000\pi t) + 20 \cos(120\pi t)
\end{align*}
\]

Find expressions for the common-mode and differential components of the input signal.

P14.4. Name the terminals of a real op amp.

**Section 14.2: Summing-Point Constraint**

P14.5. Define the term *summing-point constraint*. Does it apply if positive feedback is present?

*P14.6. List the steps in analyzing an amplifier containing an ideal op amp.

**Section 14.3: Inverting Amplifiers**

P14.7. Draw the circuit diagram of the basic inverting amplifier configuration. Give an expression for the voltage gain of the circuit in terms of the resistances assuming an ideal op amp. Give expressions for the input impedance and output impedance of the circuit.

P14.8. Consider the circuit shown in Figure P14.8. Sketch \( v_{in}(t) \) and \( v_o(t) \) to scale versus time.

*P14.9. Determine the closed-loop voltage gain of the circuit shown in Figure P14.9 assuming an ideal op amp.

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* Denotes that answers can be found on both CDs and on the web site [www.prenhall.com/hambley](http://www.prenhall.com/hambley)
P14.10. The op amp shown in Figure P14.10 is ideal except that the extreme output voltages that it can produce are ±10 V. Determine two possible values for each of the voltages shown. (Hint: Notice that this circuit has positive feedback.)

Section 14.4: Noninverting Amplifiers

P14.11. Draw the circuit diagram of the basic noninverting amplifier configuration. Give an expression for the voltage gain of the circuit in terms of the resistances assuming an ideal op amp. Give expressions for the input impedance and output impedance of the circuit.


P14.13. Each of the circuits shown in Figure P14.13 employs negative feedback. Assume that the op amps are ideal, and use the summing-point constraint. Analyze the circuits to find the value of \( v_o \) for each circuit.
P14.14. The circuit shown in Figure P14.14 employs negative feedback. Use the summing-point constraint (for both op amps) to derive expressions for the voltage gains \( A_1 = v_{o1}/v_{in} \) and \( A_2 = v_{o2}/v_{in} \).

![Figure P14.14](image)

P14.15. Analyze the ideal op-amp circuit shown in Figure P14.15 to find an expression for \( v_o \) in terms of \( v_A, v_B, \) and the resistance values.

![Figure P14.15](image)

P14.16. Analyze each of the ideal op-amp circuits shown in Figure P14.16 to find expressions for \( i_o \). What is the value of the output impedance for each of these circuits? Why? [Note: The bottom end of the input voltage source is not grounded in part (b) of the figure. Thus, we say that this source is floating.]

![Figure P14.16](image)

P14.17. Find an expression for the power gain of each of the amplifiers shown in Figure P14.17. Assume ideal op amps. Which circuit has the largest power gain?
**P14.18.** Consider the circuit shown in Figure P14.18.

- **a.** Find an expression for the output voltage in terms of the source current and resistance values.
- **b.** What value is the output impedance of this circuit?
- **c.** What value is the input impedance of this circuit?
- **d.** This circuit can be classified as an ideal amplifier. What is the amplifier type? (See Section 11.6 for a discussion of various ideal amplifier types.)

**P14.19.** Suppose that we design an inverting amplifier using 5%-tolerance resistors and an ideal op amp. The nominal amplifier gain is −2. What is the minimum and maximum gain that is possible assuming that the resistances are within the stated tolerance? What is the percentage tolerance of the gain?


**P14.21.** Consider the amplifier shown in Figure P14.21. Find an expression for the output current \(i_o\). What is the input impedance? What is the output impedance seen by \(R_L\)?

**P14.22.** Derive an expression for the voltage gain of the circuit shown in Figure P14.22 as a function of \(T\), assuming an ideal op amp. (\(T\) varies from 0 to unity, depending on the position of the wiper of the potentiometer.)

**P14.23.** Consider the circuits shown in Figure P14.23a and b. One of the circuits has negative feedback and the other circuit has positive feedback. Assume that the op amps are ideal.
except that the output voltage is limited to extremes of ±5 V. For the input voltage waveform shown in Figure P14.23c, sketch the output voltage \( v_o(t) \) to scale versus time for each circuit.

![Circuit Diagrams](image)

\[ v_{in}(t) \quad + \quad + \quad v_{o} \quad - \]

\[ v_{id}(t) \quad + \quad + \quad v_{o} \quad - \]

\[ v_{in}(t) \quad + \quad + \quad v_{o} \quad - \]

\[ +10 \quad 1 \quad 2 \quad 3 \quad \]

\[ -1 \quad -10 \quad \]

\[ t \]

**Figure P14.23**

\[ v_{in}(t) \quad + \quad + \quad v_{o} \quad - \]

**P14.24.** Repeat Problem P14.23 for the circuits of Figure P14.24a and b. (The input voltage waveform is shown in Figure P14.23c.)

![Circuit Diagrams](image)

\[ v_{in}(t) \quad + \quad + \quad v_{o} \quad - \]

\[ v_{in}(t) \quad + \quad + \quad v_{o} \quad - \]

\[ v_{in}(t) \quad + \quad + \quad v_{o} \quad - \]

**Figure P14.24**

### Section 14.5: Design of Simple Amplifiers

**P14.25.** Suppose that we are designing an amplifier using an op amp. What problems are associated with using very small feedback resistances? With very large feedback resistances?

**P14.26.** Using the components listed in Table P14.26, design an amplifier having an input impedance of at least 10 kΩ and a voltage gain of **a.** \(-10 \pm 20\%\); **b.** \(-10 \pm 5\%\); **c.** \(-10 \pm 0.5\%\).

### Table P14.26  Available Parts for Design Problems

<table>
<thead>
<tr>
<th>Part Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard 5%-tolerance resistors. (See Appendix B.)</td>
</tr>
<tr>
<td>Standard 1%-tolerance resistors. (Don’t use these if a 5%-tolerance resistor will do, because 1%-tolerance resistors are more expensive.)</td>
</tr>
<tr>
<td>Ideal op amps.</td>
</tr>
<tr>
<td>Adjustable resistors (trimmers) having maximum values ranging from 100 Ω to 1 MΩ in a 1–2–5 sequence (i.e., 100 Ω, 200 Ω, 500 Ω, 1 kΩ, etc.). Don’t use trimmers if fixed resistors will suffice.</td>
</tr>
</tbody>
</table>
P14.27. Using the components listed in Table P14.26, design an amplifier having a voltage gain of 
$-10 \pm 20\%$. The input impedance is required to be as large as possible (ideally, an open circuit).  
(\textit{Hint:} Cascade a noninverting stage with an inverting stage.)

P14.28. Using the components listed in Table P14.26, design an amplifier having a voltage gain of 
$+10 \pm 3\%$ and an input impedance of $1 \text{k}\Omega \pm 1\%$.

P14.29. Using the components listed in Table P14.26, design a circuit for which the output voltage is 
$v_o = A_1 v_1 + A_2 v_2$. The voltages $v_1$ and $v_2$ are input voltages. Design to achieve $A_1 = 5 \pm 5\%$ 
and $A_2 = -10 \pm 5\%$. There is no restriction on input impedances.

*P14.30. Repeat Problem P14.29 if the input impedances are required to be as large as possible (ideally, 
open circuits).

P14.31. A certain signal source has an internal impedance that is always less than 1000 $\Omega$ but is variable over time. 
Using the components listed in Table P14.26, design an amplifier that produces an amplified version of the internal 
source voltage. The voltage gain should be $-20 \pm 5\%$.

P14.32. Two signal sources have internal voltages $v_1(t)$ and $v_2(t)$, respectively. The internal resistances of 
the sources are known always to be less than 2 $\text{k}\Omega$, but the exact values are not known and are likely to change over time. 
Using the components listed in Table P14.26, design an amplifier for which the output voltage is 
$v_o(t) = A_1 v_1(t) + A_2 v_2(t)$. The gains are to be $A_1 = -10 \pm 1\%$ and $A_2 = 3 \pm 1\%$.

*P14.33. For Example 14.4, it is possible to achieve a design using only one op amp. Find a suitable 
circuit configuration and resistance values. For this problem, the gain tolerances are relaxed to $\pm 5\%$.

Section 14.6: Op-Amp Imperfections in the Linear Range of Operation

P14.34. The objective of this problem is to investigate the effects of finite open-loop gain, finite input 
impedance, and nonzero output impedance of the op amp on the voltage follower. The circuit including the op-amp model is shown in

Figure P14.34. \( v_o/v_s \). Evaluate for $A_{OL} = 10^5$, $R_{in} = 1 \text{ M}\Omega$, and $R_o = 25 \Omega$. 
Compare this result to the gain with an ideal op amp. \( v_o/v_s \). Evaluate for $A_{OL} = 10^5$, $R_{in} = 1 \text{ M}\Omega$, and $R_o = 25 \Omega$. 
Compare this result to the input impedance with an ideal op amp. \( v_o/v_s \). Evaluate for $A_{OL} = 10^5$, $R_{in} = 1 \text{ M}\Omega$, and $R_o = 25 \Omega$. 
Compare this result to the output impedance with an ideal op amp.

Figure P14.34

P14.35. The objective of this problem is to investigate the effects of finite gain, finite input impedance, and nonzero output impedance of the op amp on the inverting amplifier. The circuit including the op-amp model is shown in Figure P14.35. \( v_o/v_s \). Evaluate for $A_{OL} = 10^5$, $R_{in} = 1 \text{ M}\Omega$, $R_o = 25 \Omega$, $R_1 = 1 \text{ k}\Omega$, and $R_2 = 10 \text{ k}\Omega$. 
Compare this result to the gain with an ideal op amp. \( v_o/v_s \). Evaluate for $A_{OL} = 10^5$, $R_{in} = 1 \text{ M}\Omega$, $R_o = 25 \Omega$, $R_1 = 1 \text{ k}\Omega$, and $R_2 = 10 \text{ k}\Omega$. 
Compare this result to the input impedance with an ideal op amp. \( v_o/v_s \). Evaluate for $A_{OL} = 10^5$, $R_{in} = 1 \text{ M}\Omega$, $R_o = 25 \Omega$. 

Figure P14.35
$R_1 = 1 \, \text{k}\Omega$, and $R_2 = 10 \, \text{k}\Omega$. Compare this result to the output impedance with an ideal op amp.

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{circuit.png}
\caption{Op-amp model}
\end{figure}

**P14.36.** A certain op amp has a unity-gain bandwidth of $f_t = 15 \, \text{MHz}$. If this op amp is used in a noninverting amplifier having a closed-loop dc gain of $A_{0\text{CL}} = 10$, determine the closed-loop break frequency $f_{B\text{CL}}$. Repeat for a dc gain of 100.

**P14.37.** A certain op amp has an open-loop dc gain of $A_{0\text{OL}} = 200,000$ and an open-loop 3-dB bandwidth of $f_{B\text{OL}} = 5 \, \text{Hz}$. Find the open-loop gain magnitude at a frequency of \textbf{a.} 100 Hz; \textbf{b.} 1000 Hz; \textbf{c.} 1 MHz.

**P14.38.** Consider two alternatives for designing an amplifier having a dc gain of 100. The first alternative is to use a single noninverting stage having a gain of 100. The second alternative is to cascade two noninverting stages each having a gain of 10. Op amps having a gain-bandwidth product of $10^6$ are to be used. Write an expression for the gain as a function of frequency for each alternative. Find the 3-dB bandwidth for each alternative.

**P14.39.** A certain op amp has an open-loop dc gain of $A_{0\text{OL}} = 200,000$ and an open-loop 3-dB bandwidth of $f_{B\text{OL}} = 5 \, \text{Hz}$. Sketch the Bode plot of the open-loop gain magnitude to scale. If this op amp is used in a noninverting amplifier having a closed-loop dc gain of 100, sketch the Bode plot of the closed-loop gain magnitude to scale. Repeat for a closed-loop dc gain of 10.

**Section 14.7: Nonlinear Limitations**

**P14.40.** A certain op amp has a maximum output voltage range from $-10$ to $+10$ V. The maximum output current magnitude is 25 mA. The slew-rate limit is $SR = 10 \, \text{V}/\mu\text{s}$. This op amp is used in the circuit of Figure 14.28. \textbf{a.} Find the full-power bandwidth of the op amp. \textbf{b.} For a frequency of 1 kHz and $R_L = 1 \, \text{k}\Omega$, what peak output voltage is possible without distortion? \textbf{c.} For a frequency of 1 kHz and $R_L = 100 \, \text{k}\Omega$, what peak output voltage is possible without distortion? \textbf{d.} For a frequency of 1 MHz and $R_L = 1 \, \text{k}\Omega$, what peak output voltage is possible without distortion? \textbf{e.} If $R_L = 1 \, \text{k}\Omega$ and $v_i(t) = 5 \sin(2\pi \times 10^6 t)$, sketch the steady-state output waveform to scale versus time.

**P14.41.** Suppose that we want to design an amplifier that can produce a 100-kHz sine-wave output having a peak amplitude of 5 V. What is the minimum slew-rate specification allowed for the op amp?

*\textbf{P14.42.} One way to measure the slew-rate limitation of an op amp is to apply a sine wave (or square wave) as the input to an amplifier and then increase the frequency until the output waveform becomes triangular. Suppose that a 1-MHz input signal produces a triangular output waveform having a peak-to-peak amplitude of 4 V. Determine the slew rate of the op amp.

**P14.43.** An op amp has a maximum output voltage range from $-10$ to $+10$ V. The maximum output current magnitude is 25 mA. The slew-rate limit is 1 V/$\mu$s. The op amp is used in the amplifier shown in Figure P14.43. \textbf{a.} Find the full-power bandwidth of the op amp. \textbf{b.} For a frequency of 5 kHz and $R_L = 100 \, \text{k}\Omega$, what peak output voltage is possible without distortion? \textbf{c.} For a frequency of 5 kHz and $R_L = 10 \, \text{k}\Omega$, what peak output voltage is possible without distortion? \textbf{d.} For a frequency of 100 kHz and $R_L = 10 \, \text{k}\Omega$, what peak output voltage is possible without distortion?
Consider the bridge amplifier shown in Figure P14.44. a. Assuming ideal op amps, derive an expression for the voltage gain $v_o/v_s$. b. If $v_s(t) = 3 \sin(\omega t)$, sketch $v_1(t)$, $v_2(t)$, and $v_o(t)$ to scale versus time. c. If the op amps are supplied from $\pm 15$ V and clip at output voltages of $\pm 14$ V, what is the peak value of $v_o(t)$ just at the threshold of clipping? (Comment: This circuit can be useful if a peak output voltage greater than the magnitude of the supply voltages is required.)

*P14.48. Find the worst-case dc output voltages of the inverting amplifier shown in Figure 14.30a for $v_{in} = 0$. The bias current ranges from 100 to 200 nA, the maximum offset current magnitude is $50$ nA, and the maximum offset voltage magnitude is $4$ mV.

P14.49. Sometimes, an ac-coupled amplifier is needed. The circuit shown in Figure P14.49 is a poor way to accomplish ac coupling. Explain why. *(Hint: Consider the effect of bias current.) Show how to add a component (including its value) so that bias current has no effect on the output voltage of this circuit.*

P14.50. Consider the amplifier shown in Figure P14.43. With zero dc input voltage from the signal source, it is desired that the dc output voltage be no greater than 100 mV. a. Ignoring other dc imperfections, what is the maximum offset voltage allowed for the op amp? b. Ignoring other dc imperfections, what is the maximum bias current allowed for the op amp? c. Show how to add a resistor to the circuit including its value so that the effects of the bias currents cancel. d. Assuming that the resistor of part (c) is in place, and ignoring offset voltage, what is the maximum offset current allowed for the op amp?

Section 14.9: Differential and Instrumentation Amplifiers

*P14.51. Using the parts listed in Table P14.26, design a single-op-amp differential amplifier having a nominal differential gain of 10.*
P14.52. Repeat Problem P14.51 using the instrumentation-quality circuit shown in Figure 14.34.

P14.53. Consider the instrumentation-quality differential amplifier shown in Figure 14.34 with \( R_1 = 1 \text{ k}\Omega, R_2 = 9 \text{ k}\Omega, \) and \( R = 10 \text{ k}\Omega. \) The input signals are given by

\[
v_1(t) = 0.5 \cos(2000\pi t) + 2 \cos(120\pi t)
\]

\[
v_2(t) = -0.5 \cos(2000\pi t) + 2 \cos(120\pi t)
\]

a. Find expressions for the differential and common-mode components of the input signal.

b. Assuming ideal op amps, find expressions for the voltages at the output terminals of \( X_1 \) and \( X_2. \)

c. Again assuming ideal op amps, find an expression for the output voltage \( v_o(t). \)

Section 14.10: Integrators and Differentiators

P14.54. Sketch the output voltage of the circuit shown in Figure P14.54 to scale versus time. Sometimes, an integrator circuit is used as a (approximate) pulse counter. Suppose that the output voltage is \(-10 \text{ V}. \) How many input pulses have been applied (assuming that the pulses have an amplitude of 5 V and a duration of 2 ms, as shown in the figure)?

P14.55. Sketch the output voltage of the ideal op-amp circuit shown in Figure P14.55 to scale versus time.

P14.56. The displacement of a robot arm in a given direction is represented by a voltage signal \( v_{in}(t) \). The voltage is proportional to displacement, and 1 V corresponds to a displacement of 10 mm from the reference position. Design a circuit that produces a voltage \( v_1(t) \) that is proportional to the velocity of the robot arm such that 1 m/s corresponds to 1 V. Design an additional circuit that produces a voltage \( v_2 \) that is proportional to the acceleration of the robot arm such that 1 m/s\(^2\) corresponds to 1 V. Use the components listed in Table P14.26 plus as many capacitors as needed.
Section 14.11: Active Filters

*P14.57. Derive an expression for the voltage transfer ratio of each of the circuits shown in Figure P14.57. Also, sketch the magnitude Bode plots to scale. Assume that the op amps are ideal.