VLSI Digital Systems Design

Alternatives to Fully-Complementary CMOS Logic

Reasons for Alternatives

- Reasons for considering alternatives to fully-complementary CMOS logic gates
  1. Time: High speed
  2. Area: High density
  3. Power: Low power

Fully-Complementary CMOS Logic

- Ratioless
  - Works regardless of ratio of
    - impedance of pull-up network to
    - impedance of pull-down network
  - Eases design of arrays
    - Gate arrays
    - Sea of gates
- Generally, 2n transistors in n-input gate
- 2 units of load on each input

Fully-Complementary CMOS DC Current

- Virtually zero
- Useful in portable devices with standby mode
- Useful in IDDQ testing
  - Gross test
  - If there is \( I_{\text{no}} \) current when device is quiescent, assume internal fault
  - No further (expensive) testing

Alternatives 1-5 to Fully-Complementary CMOS Logic

1. Pseudo-nMOS logic
2. CMOS multidrain logic
3. Symmetric CMOS logic
4. Dynamic CMOS logic
5. Clocked CMOS logic

Alternatives 6-10 to Fully-Complementary CMOS Logic

1. Pass-gate logic
2. CMOS domino logic
3. NP domino logic
4. Cascade voltage switch logic, CVSL
5. Source follower pull-up logic, SFPL
Pseudo-nMOS Logic

- Uses pMOS transistor for pull-up
  - Has its gate permanently grounded
  - Called pseudo-nMOS for similarity to use of depletion load in nMOS logic
- Can also use constant-current source for pull-up
  - Better process tracking
- Transistor sizes must be proper ratio
  - to ensure $V_{OL}$ correct

Pseudo-nMOS Logic Circuit

Pseudo-nMOS Logic Characteristics

- Static power
  - Pull-up always on
  - Current flows when pull-down is on
- n + 1 transistors for n-input gate
  - Higher density than fully-complementary CMOS logic
- 1 unit of load on each input
  - But may want larger transistor to speed up gate

CMOS Multidrain Logic

- Electrically identical to subset of pseudo-nMOS
- In layout and logic style, related to:
  - Bipolar Integrated Injection Logic, I2L
  - or merged transistor logic
- Open drain
  - Wire together for Nor function
  - Invert and wire together for And function
  - No series transistors

CMOS Multidrain Logic Example

Symmetric CMOS Nor Gate

- Also called ganged CMOS
- Related to pseudo-nMOS logic
- Choose ratios of nMOS to pMOS to ensure correct operation
  - Best for fan-in $\leq 3$
  - 1.4 – 1.6 times faster than pseudo-nMOS Nor gate
Dynamic CMOS Logic

- When clock = 0
  - Precharge phase
  - pMOS pull-up precharges output to $V_{DD}$
- When clock = 1
  - Evaluate phase
  - nMOS pull-down network may discharge output to $V_{SS}$
  - Conversely, may use
    - nMOS pull-down to precharge to $V_{SS}$
    - pMOS pull-up network to discharge output to $V_{DD}$

Dynamic CMOS Logic Circuit Structure

Dynamic CMOS Logic Characteristics

- Active pull-up improves pull-up time
- Ground switch degrades pull-down time
  - Can eliminate ground switch by ensuring that nMOS pull-down network always off during precharge
- Inputs can only change during precharge
  - Must be stable during evaluate phase
  - Charge redistribution effects can change output charge

Cascading Dynamic CMOS Logic

- Cannot cascade single-phase dynamic CMOS logic
- During evaluate phase of second stage, first stage output is changing
- Second stage output can discharge before first stage correctly evaluates
- Dynamic CMOS logic modification for cascading
  - CMOS domino logic
  - NP domino logic, also called zipper CMOS logic
  - Two-phase logic structures
Two Stages of Dynamic CMOS Logic

![Clocked CMOS Logic](image)

- Use as interface to NP domino logic
- Use to incorporate latches
- Same input capacitance as complementary CMOS logic
- Slower due to series clocking transistors
- Series clocking transistors can be:
  - At center, as shown: faster
  - At power rails: mitigates “hot electron” effects

Clocked CMOS Logic Circuit

Pass-Gate Xnor

Pass-Gate Logic Advantages

- Fast
  - If a few stages cascaded
- Related to RC delay line
  - Delay proportional to square of number of stages

Pass-Gate Logic Disadvantages

- Complementary pass-networks desirable
  - To achieve good logic levels
  - Adds delay
- Source-drain merging more difficult
  - Compared to fully-complementary CMOS logic
  - Higher drain capacitance
- Requires both true and complement control variables
### Boolean Function Unit

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<tr>
<td>0</td>
<td>0</td>
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</table>

### Pass-Gate Boolean Function Unit

```
  P₁  | a  | ~b |
  P₂  | a  | b  |
  P₃  | a  | b  |
  P₄  | a  | b  |
```

### Pass-Gate Boolean Function Unit with Improved Layout

```
  P₁  | a  | ~b |
  P₂  | a  | b  |
  P₃  | a  | b  |
  P₄  | a  | b  |
```

### CMOS Domino Logic Circuit

```
clk --> d --> a --> b --> c --> pₚ --> z
```

### CMOS Domino Logic

- Related to clocked CMOS logic
- When clock = 0
  - Precharge phase
  - pMOS pull-up precharges pₚ output, to 1
  - Buffer output z = 0
- Evaluate phase
  - After clock = 1
  - pₚ may fall, to 0
  - Buffer output z may rise, to 1

### CMOS Domino Logic Analogy

1. At start of evaluate phase, all buffers = 0
2. Only transition possible is to rise, to 1
3. During evaluate phase, buffer will stay low until an earlier stage evaluates and rises, to 1
4. Once an earlier stage evaluates and rises, to 1, this stage evaluates.
5. If this stage rises, to 1, it will cause a subsequent stage to evaluate
   1. Analogy to a line of dominoes falling
CMOS Domino Logic Characteristics

- Can cascade any number of stages
- Twice as many logic stages
  - Inverter required
  - Inverter often needed anyway
- Can not have inverting structure
  - Can add fully-complementary logic gates after all domino logic gates
- Subject to charge redistribution
  - Can provide separate pMOS pull-ups

NP Domino Logic

- Also called zipper CMOS
- Related to CMOS domino logic
- Eliminate inverter at output of CMOS domino logic
- Successive stages alternate between
  - nMOS pull-down network, and
  - pMOS pull-up network

NP Domino Logic, Odd-Numbered Stages

- Use nMOS pull-down network
- Precharge high, to 1
- Have inputs from even-numbered stages
- Have inputs precharged low, to 0
- All nMOS in pull-down network turned off

NP Domino Logic, Even-Numbered Stages

- Use pMOS pull-up network
- Precharge low, to 0
- Have inputs from odd-numbered stages
- Have inputs precharged high, to 1
- All pMOS in pull-up network turned off
NP Domino Logic Analogy

1. During evaluate phase, buffer will stay at precharge value until an earlier stage evaluates and changes.
2. Once an earlier stage evaluates and changes, this stage evaluates.
3. If this stage changes, it will cause a subsequent stage to evaluate.

1. Analogy to a line of dominoes falling.

Cascade Voltage Switch Logic, CVSL

- Requires both true and complement versions of inputs.
  - Recall that pass-gate logic requires both true and complement control variables.
- Uses two, complementary nMOS pull-down networks.
- Each has a pMOS pull-up transistor.
- pMOS pull-ups cross-coupled.

CVSL Circuit

CVSL Positive Feedback

1. One of the two nMOS pull-down networks pulls either f or ~f low.
2. If f goes low, it turns on the pMOS pull-up transistor for the ~f totem pole,
3. causing ~f to go high,
4. turning off the pMOS pull-up transistor for the f totem pole,
5. causing f to go low: positive feedback.

CVSL Characteristics

- Slower than fully-complementary CMOS logic.
  - During switching, pMOS pull-up partially on at same time as nMOS pull-down network.
- The two nMOS pull-down networks afford opportunities to minimize logic.
  - Common sub-expression elimination.
  - Other optimizations.
- Can optimize multiple-input Xor.

CVSL 4-Input Xor Circuit
Source-Follower Pull-Up Logic, SFPL

- Related to pseudo-nMOS logic
  - Improvement: inputs control pMOS pull-up
- Inputs fed to parallel source follower
- Select ratio of $N_{load}$ to other transistors
- Any input on causes parallel source-follower output to rise
  pMOS pull-up to turn on

SFPL Circuit

SFPL Nor Gate Operation

1. Any input on causes parallel source-follower output to rise
2. Causes pMOS pull-up to turn off
3. Allows smaller nMOS pull-down network
4. Reduces output drain capacitance
5. Faster gate
6. Good for high fan-in gates

Criteria for Pseudo nMOS Logic

- Fully-complementary CMOS logic
  - Immune to noise
  - Virtually zero static power
  - Many stages required for high fan-in functions
- Pseudo nMOS logic
  - Good for high fan-in Nor function
    - ROM
    - PLA
    - Adder carry look-ahead

Criteria for Clocked CMOS and Pass-Gate Logic

- Clocked CMOS logic
  - Mitigates “hot electron” effects
- Pass-gate logic
  - Fast, if few pass gates in series
  - Good for complex functions
  - Small area, low power
Criteria for CMOS Domino Logic

- Use for high speed or low power
- Appreciate that precharge phase subtracts from cycle time
- Run circuit simulations carefully
  - Back-annotate from layout
  - Include noise effects on power and ground lines

Criteria for Cascade Voltage Switch Logic, CVSL

- Cascade Voltage Switch Logic, CVSL
  - Potentially fast
  - Large area
  - Complex
  - Susceptible to noise
- Overall rules of thumb
  - If gate resembles inverter, it will be fast
  - Pass gates, if few stages, will be fast