VLSI Digital Systems Design

- Layout of:
  - Standard Cells
  - Gate Arrays
  - Sea of Gates
  - Rules of Thumb
  - Pass Gates
  - Multiplexers

Standard Cells

- Different cells need different areas
  - Fix one dimension: height
    - VDD and VSS busses traverse the cell
    - At top and bottom
    - Connect by abutment
    - Internal area for connecting transistors
  - Vary width
  - Also called polycells

Standard Cell Transistor Sizing

- All pMOS same size: maximum allowed
- All nMOS same size: maximum allowed
- Further optimization:
  - Adjust individual transistor sizes
  - Larger transistors
    - Pro: Larger drive
    - Con: Larger input and output capacitance, area
  - Smaller transistors
    - Con: Smaller drive
    - Pro: Smaller input and output capacitance, area

Standard Cell with Reduced nMOS Capacitance

Standard Cell with Metal2 Ports
Gate Arrays

- Fixed layers
  - Well
  - Diffusion
  - Polysilicon
- Programmed layers
  - Contact
  - Metal1
  - Via
  - Metal2

Gate Array Cell Site

```
    **      **      **
dd**ddaadd**dbbadd**ddccdd**dddddddieddd-Vdd
aa  bb  cc
pppp--pppppp--pppppp--pppppp
**pp--pp**pp--pp**pp--pp**
pppp--pppppp--pppppp--pppppp
aa  bb  cc
```

Programmed Gate Array Cell

```
    **      **      **
dd**ddaadd**dbbadd**ddccdd**dddddddieddd-Vdd
mm  aa  bb  mm  cc
mmmm--mmmm--mmmm--mmmm--mmmm
**nn--nn**nn--nn**nn--nn**
mmmm--mmmm--mmmm--mmmm--mmmm
mm  aa  bb  cc
ss**ssaass**ssbbss**ssccss--ssssssssssssssssss-Vss
**      **      **
```

Gate Array Parameters

- For all chips:
  - Fixed number of transistors in each logic cell
  - Fragmentation if need fewer in a logic cell
  - Can gang cells
  - Fragmentation if need fewer than even multiple
  - Fixed transistor size
  - Fixed number of tracks in routing channel

Sea of Gates

- Continuous row of nMOS across master chip
- Continuous row of pMOS across master chip
- Consume one transistor-pair site to isolate logic gate from its neighbor
  - Tie pMOS transistor gate to VDD
  - Tie nMOS transistor gate to VSS
- Also called CMOS Cell Array

Sea of Gates Advantages

- Logic gate cells are variable in size
  - Consume transistor pair to isolate logic gate
  - No need to set as parameter for all chips
- Devote area to gates or routing as required
  - Route over unused transistors
  - No need to set as parameter for all chips
Sea of Gates Transistor Array

Programmed Sea of Gates

Layout Rules of Thumb, Page 1

- Timing Rules of Thumb, cmpe222_05full_complement_ppt.ppt, pages 12 and 13
- Run \( V_{DD} \) in metal at top of cell
- Run \( V_{SS} \) in metal at bottom of cell
- Run gate input in polysilicon vertically for each transistor

Layout Rules of Thumb, Page 2

- Create diffusion segments by ordering transistors to maximize source-drain connections by abutment
- Place pMOS segments close to \( V_{DD} \)
- Place nMOS segments close to \( V_{SS} \)
- Minimize internal node capacitance

Transistor-Level v. Gate-Level

- 10 – 100 transistor logic block
- 25 – 75 % reduction in area
- More source-drain connections by abutment
- Less fragmentation
- Labor intensive
  - Reserve for frequently-occurring structures
    - Standard cells
    - Datapath

Minimize Output Drain Capacitance

- If you have a choice to connect parallel transistors either to:
  - output, or
  - \( V_{DD} \) or \( V_{DD} \)
- Choose source-drain connections by abutment to connect to output
- Minimize output drain capacitance
  - Faster gate
- Maximize \( V_{DD} \) or \( V_{DD} \) capacitance
Success at Minimizing Nor Output Drain Capacitance
**dddddddddddddddddddddddddddddddddddddddd-Vdd**
**pp--pp**
Z
aa mm bb
**nn--nn**
ss aa bb
**ssssssssssssssssssssssssssssssssssssssssssss-Vss**
A-aa B-bb

Success at Minimizing Output Drain Capacitance
**dddddddddddddddddddddddddddddddddddddddddd-Vdd**
**pp--pp**
Z
aa mm bb
**nn--nn**
ss aa bb
**ssssssssssssssssssssssssssssssssssssssssssss-Vss**
A-aa B-bb C-cc D-ee

Pass Gate Layout
1. Minimal area
   - No horizontal metal pass-through
2. Allow horizontal metal pass-through
   - Larger area
3. Allow horizontal metal pass-through
   - Using metal2
Route Select Signals to Array

1. Run horizontally in metal, outside transistors
2. Run vertically in polysilicon
3. Run vertically in polysilicon strapped by metal1

Pass Gate with Select Run Outside

Pass Gate with Offset Transistors

Pass Gate with Poly-Metal1 Strap

Pass Gate Layout w Metal Pass-Throughs

Pass Gate Layout w Pass-Thru Using Metal2
Multiplexer Select Lines

1. Select lines continuous
2. Select lines crossed inside
3. Select lines crossed outside

Multiplexer with Continuous Select Lines

Multiplexer with Crossed Select Lines

Multiplexer with Select Crossed Outside

Multiplexer with Continuous Select Lines

Multiplexer with Crossed Select Lines

Multiplexer with Select Crossed Outside