VLSI Digital Systems Design

Circuit and Physical Design of Fully-Complementary CMOS Logic Gates

Fan-in

- Fan-in = number of inputs to a gate
- Examples:
  1. Nand g1 (outg1, in1, in2, in3, in4); fan-in = 4
  2. Nor g2 (outg2, in1, in2); fan-in = 2

Fan-out

- Fan-out = number of inputs that a gate's output drives
- In units of minimum-sized inverters
- Examples:
  - Nand g1 (outg1, a, b, c, d);
  - Nor g2 (outg2, a, e);
  - Not g3 (a, f); fan-out = 2

Large Fan-in Slows Gate

- Resistance of series transistors in pull-up network or pull-down network additive
- Two transistors in series will double the rise or fall time compared to single transistor

Worst-case delay time

- $T_{df} = \text{worst-case fall delay time}$
- $T_{df} = t_{\text{internal-f}} + k \cdot t_{\text{output-f}}$
- $T_{dr} = \text{worst-case rise delay time}$
- $T_{dr} = t_{\text{internal-r}} + k \cdot t_{\text{output-r}}$
- where $k = \text{fan-out}$
  - in units of minimum-sized inverters

Gate Delays

- Delay $t_{\text{internal-f}}$, $t_{\text{output-f}}$, $t_{\text{internal-r}}$, $t_{\text{output-r}}$
- Units ns, ns/pF, ns, ns/pF
- Gate
  - INV 0.08 1.70 0.08 2.10
  - ND2 0.20 3.10 0.15 2.10
  - ND4 0.68 5.70 0.25 2.10
  - ND8 2.44 9.99 0.38 2.20
  - NR2 0.14 1.75 0.25 4.10

8-input And, Case 1

- Nand stage1 (s1out, a, b, c, d, e, f, g, h);
- Not stage2 (s2out, s1out);

8-input And, Case 2

- Still 2 stages
- Less fan-in

8-input And, Case 3

- Twice as many stages
- Minimal fan-in
8-input And, Comparison

<table>
<thead>
<tr>
<th>Stage</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>Total</th>
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<tr>
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<td>fall</td>
<td>rise</td>
<td>fall</td>
<td>rise</td>
<td>Delay</td>
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<td>2.18</td>
<td>0.00</td>
<td>0.00</td>
<td>4.62</td>
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<tr>
<td>2</td>
<td>0.68</td>
<td>4.35</td>
<td>0.00</td>
<td>0.00</td>
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<tr>
<td>3</td>
<td>0.20</td>
<td>0.25</td>
<td>0.20</td>
<td>2.18</td>
<td>2.83</td>
</tr>
</tbody>
</table>

Transistor Sizing

1. Start with minimum-sized devices
2. Determine critical paths
3. Increase the gate size along critical paths

Timing Rules of Thumb, Page 1

- Use Nands
- Avoid Nors
- Output rise and fall time depend on input rise and fall times
  - Keep edges sharp throughout each critical path

Timing Rules of Thumb, Page 2

- Keep fan-out low
  - Below 5-10
  - Use minimal-sized gates to minimize the load on gates with high fan-out
  - Drive high fan-out nets with inverters
- Keep fan-in low
  - Unless low power or low area is more important

Layout Layer Key

- aa = poly (input)
- bb = poly (input)
- cc = poly (internal)
- mm = metal (internal)
- dd = Vdd (metal)
- ss = Vss (metal)
- nn = n-diffusion
- pp = p-diffusion
- -- = gate
- ** = contact

Vertical-Transistor Inverter Layout

Horizontal-Transistor Inverter Layout

Central Metal Pass-Through

Top & Bottom Metal Pass-Thru
Large-Transistor Inverter Layout

Back-to-Back-Transistor Inverter Layout

Advantages of Back-to-Back-Transistor Inverter Layout

• Drain area does not increase in size much
  – Drain capacitance does not increase much
• Transistor gain doubled

Advantages of Doughnut-Transistor Inverter Layout

• Drain area does not increase in size much
  – Drain capacitance does not increase much
• Transistor gain almost quadrupled
• Also called “round transistor” connection

“Line of Diffusion” Layout

• Single row of p-transistors above single row of n-transistors
• Aligned at common gate connections
• Transistors form line of diffusion intersected by polysilicon gate connections
• All complementary gates can be designed this way
• Most simple gates can be designed without a break in the diffusion

Complex Gate Layout

• Convert circuit to two graphs
  1.p-transistor pull-up network
  2.n-transistor pull-down network
• Each graph is the dual of the other
• Vertices = source-drain connections
• Edges = transistors that connect vertices
  – Labeled with gate signal name for that transistor

Euler Path

• If two edges are adjacent in one of the graphs
  – They share a common source-drain connection
  – They can be connected by abutment
• If there is an Euler path
  – if there is a sequence of edges
    • containing all edges in the p-graph and the n-graph
    • that have identical labeling
    – then the gate can be designed with no breaks

“Line of Diffusion” Layout Algorithm

1. Find all Euler paths that cover the n-graph and the p-graph
2. Find an Euler path for the n-graph and an Euler path for the p-graph that have identical labeling
   • labeling = ordering of the gate labels on each vertex
3. If not found, break the gate in the minimum number of places to achieve step 2 by separate Euler paths
Stacked Transistor Layout

- Input signal applied to gates of multiple transistors
- Transistors stacked on appropriate gate signal
- Used for cascaded gates
- Xnor
- Variation in distance between power lines makes standard cell layout more difficult
  - C.f. "line of diffusion" layout

Xnor Logic

\[ \text{Xnor}: \quad z = \text{a Xnor b} \]

Hand portion of "line of diffusion" Xnor Layout

```
Vss | Vdd
---+---
ss  | dd
ss  | dd
ss  | dd
ss  | dd
ss  | dd
ss  | dd
ss  | dd
ss  | dd
ss  | dd
ss  | dd
```

Hand portion of "line of diffusion" Xnor Layout

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Vss | Vdd
---+---
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ss  | dd
ss  | dd
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```

Hand portion of Stacked-Transistor Xnor Layout

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Vss | Vdd
---+---
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ss  | dd
ss  | dd
ss  | dd
ss  | dd
ss  | dd
ss  | dd
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ss  | dd
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```

Stacked-Transistor Xnor Layout

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Vss | Vdd
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