VLSI Digital Systems Design

Process Enhancements and Design Rules
Metal Layer Enhancements

• Additional metal layers easier to route
• May require separation between via and contact cut
  – Bridged with metal-1 tab
• May require metal borders around via on both levels
Polysilicon + Refractory Metal

- 20 < R of doped polysilicon < 40 Ω/square

1. Silicide gate
   - Combine polysilicon with refractory metal
   - E.g., tantalum
   - 1 Ω/square < R < 5 Ω/square

2. Polycide
   - Layer of silicide on top of
   - Layer of polysilicon

3. Salicide
   - Self aligned polysilicon + silicide
Local Interconnect

• Use silicide for short-distance interconnect
  – Within a cell
  – E.g., TiN
• Less area
  – No need for contacts
  – No need for metal
Resistors

- Undoped polysilicon
  - Mask poly during implant step
- Tera Ωs
- SRAM
- Can laser-trim for accuracy
Capacitors

• Used in switched-capacitor analog
  – Extra layer of polysilicon
  – Poly-thinox-poly sandwich
  – 10 nm < thin SiO₂ < 20 nm

• Used in DRAM
  – 3-D structure = trench capacitor
Flash Memory

• Extra polysilicon layer
  1. Control gate, above...
  2. Inter-poly oxide, above...
  3. Floating gate, above...
  4. Tunnel oxide, above...
  5. Channel

• Fowler-Nordheim current tunnels through thin tunnel oxide to floating gate to program the cell
Well Rules

• Active cannot cross a well boundary
  – To avoid a shorted condition
• Put a substrate contact wherever space is available
  – Since n-well sheet resistance can be several KΩ/square
Figure 2.15. Design rules which determine the separation between the nMOS and the pMOS transistor of the CMOS inverter.
Transistor Rules

• Poly must completely cross diffusion
  – Otherwise diffusion short-circuits the transistor
• Require poly to extend beyond diffusion
  – Diffusion expands beyond initial region
• Called gate extension
Gate Extension, Channel L & W

*Figure 2.14.* Design rules which determine the dimensions of a minimum-size transistor.
Metal-1 Rules

• Wider metal lines may require more spacing
  – Called fat-metal rules
  – Caused by etch characteristics of different-width metal wires
• May be maximum metal width
• May be maximum parallel metal length
• May require proportion of chip covered with metal
  – Manufacturability
Via Rules

• May allow vias over poly and diffusion
• May allow vias over poly and diffusion, but not over boundary
  – Planarity
• May allow vias over vias
• May require separation between via and contact cut
Metal-2 Rules

• May differ from metal-1 rules
• Upper layers have greater planarity concerns
  – Step coverage
• Increase in width rules
• Increase in separation rules
• Top metal layers (can be 6-8) usually reserved
  – Power supply
  – Clock distribution
Antenna Rule Situation

• Polysilicon and metal
  – Connected to gate at one end
  – Floating at other end
• Reactive ion etch
  – Collects charge
  – Large potential develops
• Fowler-Nordheim current tunnels through thin oxide to gate
• Also called process-induced damage
Antenna Rule Result

• May result in either
  – Reduced transistor performance, or
  – If antenna rules seriously violated, total failure

• Antenna ratio of
  – Exposed conductor area to
  – Transistor gate thin oxide area
  – Must be less than a process-dependent limit
Scaling

• As process improves, finer feature size becomes possible
• Not all design rules scale together
• Strictly speaking, redesign required
• Scaling without redesign can take advantage of improved process to some degree
Latchup

• Parasitic vertical PNP in n-well
  – P = diffusion
  – N = n-well
  – P = p-substrate

• Parasitic horizontal NPN in p-substrate
  – N = diffusion
  – P = p-substrate
  – N = n-well
Inequality for Latchup to Occur

- $\beta_{nnp} \times \beta_{pnp} > 1 + \frac{\left( \beta_{nnp} + 1 \right) \times (I_{Rsubstrate} + I_{Rwell})}{(I_{DD} - I_{Rsubstrate})}$

- Latchup prevention:
  1. Reduce gain of parasitic transistors
  2. Reduce resistor values
Latchup Prevention by Process

• Thin epitaxial layer on top of highly-doped substrate
  – Use for starting material
  – Reduces gain of parasitic transistors

• Retrograde well structure
  – Highly doped at bottom of well
  – More lightly doped at top of well
  – Reduces well resistance deep in well
Latchup Prevention by Layout

- Liberal substrate and well contacts
  - Reduce $I_{R_{\text{substrate}}}$
  - Reduce $I_{R_{\text{well}}}$
- Substrate contact in every well
- Metal (no poly) interconnect from substrate contact to IO pad
- Substrate contact every 5-10 transistors
- Guard rings spoil parasitic transistor gain
  - Area penalty. Use on proven IO structures