CMOS Digital System Design

MOS Transistor DC Operation
Threshold Voltage $V_t$

- $V_{gs} < V_t$: nMOS channel is cut off
- $V_t < V_{gs}$: nMOS channel conducts
- $V_{gs} < V_t$: pMOS channel conducts
- $V_t < V_{gs}$: pMOS channel is cut off
Enhancement Mode Transistors
Depletion Mode Transistors

• Enhancement mode:
  channel is cut off when $V_{gs} = 0$

• Depletion mode:
  channel conducts when $V_{gs} = 0$

• Most CMOS ICs use enhancement-mode transistors.
n-MOS Channel Layers, Page 1

• When $V_{gs} = 0$, drain-to-substrate is reverse-biased $pn$ junction.

• When $V_{gs} > 0$, positive electric field in channel under gate:
  – repels holes
  – attracts electrons
n-MOS Channel Layers, Page 2

• When $V_{gs} \ll V_t$:
  – Mobile positive holes in p-type channel in substrate are evenly distributed.
  – Called accumulation layer

• When $V_t < V_{gs}$:
  – Holes are repelled, causing a depletion region under the gate.
  – Called depletion layer
n-MOS Channel Layers, Page 3

• When $V_t \ll V_{gs}$:
  – Electrons are attracted, causing a conductive layer under the gate.
  – Called inversion layer
n-MOS Operating Regions, Page 1

• When $V_{ds} = 0$:
  – Depletion and inversion layers uniform depth along length of channel

• When $V_{ds} > 0$:
  – Depletion and inversion layers same depth at source end of channel as for $V_{ds} = 0$
  – Inversion layer tapers off linearly toward drain end
n-MOS Operating Regions, Page 2

• When $V_{ds} < V_{gs} - V_{t}$:
  – Inversion layer becomes deeper as $V_{gs}$ increases
  – $I_{ds}$ depends on both $V_{gs}$ and $V_{ds}$.
  – Called linear region.
  – Also called resistive region.
  – Also called nonsaturated region.
  – Also called unsaturated region.
• When $V_{ds} > V_{gs} - V_t$:
  – $V_{gd} < V_t$.
  – Inversion layer pinched-off: no longer reaches drain from source end of channel
  – Electrons instead injected into depletion layer, then accelerated toward drain
  – $I_{ds}$ depends only on $V_{gs}$, independent of $V_{ds}$.
  – Called saturated region
Body Effect

- When have series-connected nMOS devices, only the bottom one has source connected to GND.
- Others have $V_{sb} = (V_{source} - V_{substrate}) > 0$
- For those, have greater gate-channel voltage difference
- Increase in $V_t$. 
Cutoff Region DC Equation

- For $V_{gs} \leq V_t$:
- $I_{ds} = 0$
Nonsaturation Region DC Equation

• For $0 < V_{ds} < V_{gs} - V_t$:
  
  $$I_{ds} = \text{Beta}((V_{gs} - V_t)V_{ds} - V_{ds}**2 / 2)$$

• Beta = MOS transistor gain factor
Saturation Region DC Equation

- For $0 < V_{gs} - V_t < V_{ds}$:
  
  $I_{ds} = \frac{\text{Beta}(V_{gs} - V_t)^2}{2}$

- Beta = MOS transistor gain factor
  
  $= \left( \frac{(\mu)(\epsilon)}{t_{ox}} \right)(W/L)$

- mu = channel carrier mobility

- epsilon = gate insulator permittivity (SiO$_2$)

- $t_{ox}$ = gate insulator thickness

- $W/L$ = channel dimensions
LOW Noise Margin

- $V_{IL}$ = LOW input voltage
- $NM_L$ = LOW noise margin
- Unity gain point, slope = -1
  - $V_{IL}$ = 2.3 volts
  - $NM_L$ = 2.3 volts
HIGH Noise Margin

- $V_{IH} = $ HIGH input voltage
- $NM_H = $ HIGH noise margin
- Unity gain point, slope = -1
  - $V_{IH} = 3.3$ volts
  - $NM_H = 1.7$ volts
Differential Amplifier, Page 1

• Pair of nMOS transistors, each with a pull-up resistor
• Sources connected through constant-current source to ground
Differential Amplifier, Page 2

- If $V_{in1}$ and $V_{in2}$ change equally from $V_{\text{quiescent}}$, $V_{out1}$ and $V_{out2}$ stay the same.

- If only $V_{in1}$ changes:
  - current changes one way in resistor 1 and the other way in resistor 2
  - So $V_{out1}$ changes one way and $V_{out2}$ changes the other.
Differential Amplifier, Page 3

- Common Mode Gain low
- Differential Gain high
- CMRR = Common Mode Rejection Ratio
  = Differential Gain/Common Mode Gain
- Good for rejecting common mode noise on input pins
- Used in RAM sense amplifiers
Current Mirror

- Pair of nMOS transistors with gates tied together
- Tie drain of side device to its gate to put it in saturation
- Feed constant current in side transistor
- Identical current will flow in other transistor, since they are in saturation and $V_{gs1} = V_{gs2}$. 
Tri-State Driver

- Inverter followed by a pass gate
- For same size n- and p-devices, half the speed of inverter alone
- Can omit connection between inverter devices
- Used in bus drivers and latches
- Can be drawn as one gate
- (“Tri-State” is a registered trademark of National Semiconductor Corporation.)
Junctions and Diodes

• At $pn$ junction, junction diode formed
• At metal-semiconductor junction, creates either:
  – Ohmic contact, or
  – Schottky diode (used extensively for high-frequency, low-noise mixer and switching circuits).
  – Only ohmic in most CMOS processes
Diode DC Equation

\[ I = A_d I_s (\exp(qV/kmt) - 1), \]

where:

- \( I \) = current in a diode
- \( A_d \) = area of the diode
- \( I_s \) = the saturation current/unit area
- \( q \) = the charge of an electron
- \( k \) = Boltzmann's constant
- \( t \) = temperature
- \( m \) = approx. 2.0 for \( pn \)-junction diodes, and
  - \( m \) = approx. 1.2 for Schottky diodes
BiCMOS Drivers

• With extra processing steps added to a CMOS process, can build useful NPN transistors
• NPN has high current gain
• Can improve output drive of CMOS inverter