Computer Engineering 222.
VLSI Digital System Design

Introduction
Related Courses, Page 1

- 171 Analog Electronics
- 226 Computer-Aided Analysis of Electrical Circuits
- 178 Device Electronics
- 228 Semiconductor Fabrication Technology
- 100 Logic Design
• 225 Introduction to ASIC Systems Design
  – Behavioral design specification
  – System partitioning
  – Synthesis tools
  – Design verification
Related Courses, Page 3

- 227 Advances in Computer-Aided Synthesis of VLSI Circuits
- 232 Arithmetic Processors
- 224 Testing Digital Circuits
MOS Transistors, Page 1

• Metal-Oxide-Silicon structure
  – Gate
    • Conducting electrode (not actually metal) over variable-conductivity channel
  – Insulator
    • Silicon dioxide
  – Variable-conductivity channel
    • crystalline Silicon
MOS Transistors, Page 2

- One diffused region forms the source terminal
- The other, the drain
- nMOS transistor = n-type regions diffused into p-type substrate
- pMOS transistor = p-type regions diffused into n-type substrate
MOS Transistor Switches

• nMOS
  – Conducts when gate is high
  – Off when gate is low

• pMOS
  – Conducts when gate is low
  – Off when gate is high
Pass Gate

- Place an nMOS transistor in parallel with a pMOS transistor
  - Drive nMOS with signal $S$
  - Drive pMOS with signal $\text{Not } S$
- Passes 0s and 1s acceptably when $S$ is high
  - But does not restore levels, so can’t cascade
- Also called transmission gate
- Also called complementary CMOS switch
MOS Inverter

• Can make inverter with either:
  – Open-drain pMOS with pull-up resistor, or
  – Open-source nMOS with pull-down resistor

• Advantages of MOS over CMOS
  – No need for well for complementary MOS transistors, so fewer masks and process steps, so lower cost.
  – Fewer chances for defects, so higher yield.

• Disadvantages of MOS over CMOS
  – If choose high-impedance pull-up resistor, output is slow to pull up
  – If choose low-impedance pull-up resistor, gate is power hog. VLSI chip requires heroic cooling.
CMOS Inverter

- Fast to pull up, fast to pull down
- Virtually zero static power
- Restores logic levels, so can cascade
- Disadvantage over MOS: more masks and process steps
CMOS Nand

• Like inverter:
  – pMOS pull-up tree
  – nMOS pull-down tree

• pMOS devices in parallel
  – if A=0 or B=0, then out=1 (see Karnaugh)

• nMOS devices in series
  – if A=1 and B=1, then out=0
CMOS Nor

- Like inverter and Nand:
  - pMOS pull-up tree
  - nMOS pull-down tree
- pMOS devices in series
  - if $A=0$ and $B=0$, then $out=1$
- nMOS devices in parallel
  - if $A=1$ or $B=1$, then $out=0$
Compound gates, Example 1

- $F = \text{Not } (AB + CD)$
- Form pMOS pull-up tree from $F$
  - In terms of the Not of each input
  - $(\text{Not } A + \text{Not } B)(\text{Not } C + \text{Not } D)$
- Form nMOS pull-down tree from Not $F$
  - In terms of the true sense of each input
  - $(AB + CD)$
Compound gates, Example 2

- \( F = \neg ((A + B + C)D) \)
- Form pMOS pull-up tree from \( F \)
  - In terms of the \( \neg \) of each input
  - \((\neg A)(\neg B)(\neg C) + \neg D\)
- Form nMOS pull-down tree from \( \neg F \)
  - In terms of the true sense of each input
  - \((A + B + C)D\)
Pass-gate Mux

• Implement Out = AS + B(Not S)
• Pass A through a first pass gate
  – Drive nMOS with signal S
  – Drive pMOS with signal Not S
• Pass B through a second pass gate
  – Drive nMOS with signal Not S
  – Drive pMOS with signal S
• Connect the two pass gates’ outputs
  – Does not restore levels, so don’t cascade
Transparent Latch

• Two inverters in feedback loop
• Their input driven by either:
  – Pass gate (take care with drive strength), or
  – Mux between input and feedback
• Output follows input for one phase of clock
• Also called level-sensitive latch
Edge-triggered, master-slave register

• Back-to-back latches
• First stage = master
  – Clocked on one phase of clock
  – Its output follows register’s input
• Second stage = slave
  – Clocked on other phase of clock
  – Its output only changes on clock edge
• Also called D register
• Also called D flip-flop
Degree of Detail in Design Representation

• Behavioral
• Structural
• Physical
Behavioral Representation

- Cycle-accurate
- Gates unspecified
- Cycle time unspecified
- Languages:
  - Verilog RTL
  - VHDL
  - System C
Structural Representation

- Gate interconnections specified
- Gate types (And, Or) specified
- Initial gate strengths specified
- Enables initial estimates of area, power, and timing
- Languages:
  - Verilog netlist
  - Spice netlist
  - LSI Logic netlist
Physical Representation

• Placement specified. Enough information to enable:
  • Interconnect length and path
  • Best timing information
  • Exact area required
  • Design Rule Check
  • Tape Out
    – Language: GDS-II
Design Flow

• Data sheet specification
• Behavioral representation
  – Verify that function is the same
• Structural representation
  – Verify that function is the same
• Physical representation
  – Verify that function is the same
  – Check timing, power, design rules