MWF: 12:30pm – 1:40pm  
Lecture room: BE 156  
Laboratory room: BE 340

Instructor: Cyrus Bazeghi  
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Office: E2-319  
Office Hours: 2pm – 3pm MWF and by appointment  
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Important dates:
Midterm is on Friday, October 21st  
Final is on Tuesday, December 6th from noon to 3pm

Required Textbook:
ISBN: 0-13-061970-1

Optional Textbook:

Web sites:
Class web site: http://www.soe.ucsc.edu/classes/cmpe222/Fall05/  
Check this site regularly for announcements and handouts. It will evolve over the course of the quarter  
Discussions web site: http://apps.soe.ucsc.edu/forums/  
Use this to have discussions between yourselves. If questions to the instructor are posted please also use email also so a timely response can be made.

Course Work:
Welcome to CMPE222, I hope you get a lot out of this class, I feel it can be one of the most relevant and practical classes (besides being fun and interesting) available in computer engineering at UCSC.

In this course we will cover the fundamental topics necessary to successfully engineer modern VLSI designs in an ASIC (application specific integrated circuit) flow. This requires that we investigate two overlapping areas of study. The first gives students a review of fabrication technologies and device physics. This involves learning how modern integrated circuits are manufactured and what their electrical properties are. We will cover the principles of full custom layout and how to simulate and verify them.
From this base we will progress to a study of how to implement combinational and sequential logic in a hardware description language (HDL) such as Verilog. This topic includes: basic combinational blocks, arithmetic units, flip-flops and latches, clocks, and synchronous and asynchronous state machines and interfaces.

The second area of study deals with how to go from various functional descriptions of digital systems to actual silicon implementations. Here we learn the tools and techniques needed to translate, optimize, place, route, measure timing and power, and produce a fabrication ready GDSII output. This will be done in a very practical and hands-on way using very modern industry grade EDA (electronic design automation) tools.

You will be given weekly homework and lab assignments. I strongly suggest you take them seriously as they will prepare you for the exams, count the most toward your grade and keep you in synch with the lectures as we will build upon material over the entire quarter. You should try to do the assignments first independently before consulting other students for aid. Appropriate aid is a friend/colleague showing you how to do the problem, not doing the problem for you. You are not allowed at anytime to simply copy someone else’s assignment. If collaboration was done you must put the person’s name on your assignment or in your source.

Academic honesty is a requirement for the course. Cheating on the midterms or final will result in failure in the course (class and lab) and you will be reported to your department.

If you have any disability-related needs, be sure to contact the Disability Resource Center and the instructor well in advance of any expected need.

Evaluation:

The evaluation criteria for CE222 will be homework & lab assignments (50%), exams (25%), final project (20%), and attendance and participation (5%).

Labwork:

A major goal of this course is to give you relevant and modern exposure to VLSI design flows. There are MANY tools and MANY combinations that are used in the industry. I have chosen a selection of tools that I feel are a good balance between cutting edge and relative ease of learning the basics. It is hoped that you will learn enough from this course and lab experience to confidently say you can use the tools presented in a moderately competent way.

You are encouraged to keep a proper chronologically ordered engineering notebook that will be used along with your lab demonstrations as the evaluation criteria. The notebook will contain your complete lab report write-up if requested plus all engineering notes. More information on this will be covered in class.

You will be allowed to work with a partner and discussions between groups are allowed though sharing of work is not. You are expected to keep your own notebook and are required to be able to demo and explain the entire lab assignment with out aid of your partner. You do no service to your friend if you do all the work and just let them copy.

With most engineering you learn by doing, not by reading or listening. You will be expected to put a fairly considerable amount of time working on learning and using the various EDA tools that will be presented to you. The instructor has gone to a lot of pains to obtain training material and documentation to help you as much as possible but much time will be spent “figuring out” how things work. This is VERY typical of a real world job in ASIC design as tools and techniques constantly change.