The L-2 cache has a 2% miss rate and D-cache blocks, and the D-cache is composed of a split L1 cache that eliminates stall for accessing off-chip memory through a 5% miss rate and L6-byte blocks. There is a write-through mechanism for this computer. Exercise 5.2 on a Sun Blade 1000.

\[ \text{L1 = 64 B, L2 = 128 K, } L2 = 6.9 \times 10^4 \]

Legend (power of 2):
- **128K**
- **64K**
- **4K**
- **2K**
- **1K**
- **512**
- **256**
- **128**
- **64**
- **32**
- **16**
- **8**
- **4**
- **2**

The results show a curve with a peak at approximately L2 = 6.9 x 10^4.
compaction = ~2-3x saam cell