Timers and Analog to Digital Conversion:
Tick tock tick tock...

Gabriel Hugh Elkaim
2015
Interfacing to the Real World

The world

Sensors

ADC

I/O ports

Timers

Communication

PWM

I/O ports

Communication

DAC
Timers

Counter

String of flip-flops

counter driven by a fixed clock input
Controller - medium complexity - 5 16-bit units

Dedicated chips (SPIs)

RTCC ~ 1 man/year

GPS - pps \uparrow

< 1 man/year
Carter Fige can vary 86.5

Crown Pulst - Pcy

Annotated Mechanism

12 rpm

0 - 255

0 - 5387

0 - 66,111

5 mm Tcx0

OCX0

TMRx

PRx

1 ppm

CMPE 118/218 - Intro. to Mechatronics
Software Things

ES_Things

— Thin 2, Roller

16 individual chains

Free Hanging Thin (1) —

ES_Thine_CoolThin (1) ;
Figure 16-1: Output Compare Module Block Diagram
Elapsed time indicator

Cycled timer

[Diagram of a timer with steps and a line graph indicating elapsed time]
Software Timers

$T_{38}$-loops

Timers.hi()}

16 software timers
PWM Mode

Duty Cycle: $\frac{\text{High Time}}{\text{Period}} \times 100$

$f = \frac{1}{\text{Period}}$
Figure 15-1: Input Capture Module Block Diagram
Measuring time between events

\[ \text{arc} \quad \frac{157 - 157}{32} \quad \text{trm} \quad 80 \text{mm} \]

\[ F_{PB} - F_{MV_2} = 80 \times 10^2 \quad \text{cm} - \text{cm} \]

\[ \frac{98 \times 10}{2} \]
PWM - Drive Motors

\[ \Rightarrow D.C. \]

Left edge aligned

Right edge aligned (BLDC)
Analog-to-Digital Conversion

Figure 17-1: 10-bit High-Speed ADC Block Diagram

Succession Approximation Register

Note 1: VREF+ and VREF- inputs can be multiplexed with other analog inputs.
Figure 17-5: Simplified 10-bit High-Speed ADC Block Diagram for Alternate Sample Mode
Analog Voltage

High Time x Analog Voltage

Result

Single Mode ADC
Diagram showing a circuit with labeled parts:
- Input signal
- Charge
- Double Slope ADC
Sun work.

78 kN3.
ΔΣ

\[ V_{in} \rightarrow \int \rightarrow \text{DAC} \rightarrow X \rightarrow Y \rightarrow U_{ref} \]

Accuracy \sim 24 \text{ bit}

\( V_{ref} \sim 1000 \text{ mV} \)
### Conversion Code

<table>
<thead>
<tr>
<th>Range of Analog Input Values</th>
<th>Digital Output Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>45 - 5.5</td>
<td>0 ... 101</td>
</tr>
<tr>
<td>35 - 4.5</td>
<td>0 ... 100</td>
</tr>
<tr>
<td>25 - 3.5</td>
<td>0 ... 011</td>
</tr>
<tr>
<td>15 - 2.5</td>
<td>0 ... 010</td>
</tr>
<tr>
<td>05 - 1.5</td>
<td>0 ... 001</td>
</tr>
<tr>
<td>0 - 0.5</td>
<td>0 ... 000</td>
</tr>
</tbody>
</table>

**Elements of Transfer Diagram for an Ideal Linear ADC**

- Ideal Straight Line
- Step Width (1 LSB)
- Midstep Value of 0 ... 011
- Quantization Error
- Inherent Quantization Error (± 1/2 LSB)
$y(t)$ sampled at $\Delta t$
Claude Shannon — $\frac{25}{2}$

Anti-Shaking Filter —

44.1 kHz, 96 kHz.

Least analog part in a system.
Comparator

Figure 19-1: Comparator Block Diagram

Note 1: On devices with a USB module, and when the module is enabled, this pin is controlled by the USB module, and therefore, is not available as a comparator input.

2: Internally connected.
Comparator (2.2)
Comparator Voltage Reference

Figure 20-1: Comparator Voltage Reference Block Diagram

Note 1: These bits are not available on all devices. On such devices, CVREF is generated by the resistor network and IVREF is connected to 1.2V. Refer to the specific device data sheet for availability.
$5$ levels

\[ \frac{1}{2} \text{ LSB} \quad \text{Step Height (1 LSB)} \]

\[ \frac{1}{2} \text{ LSB} \quad \text{Step Value} \]

**CONVERSION CODE**

<table>
<thead>
<tr>
<th>Digital Input Code</th>
<th>0...000</th>
<th>0...001</th>
<th>0...010</th>
<th>0...011</th>
<th>0...100</th>
<th>0...101</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Output Value</td>
<td>0</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>5</td>
</tr>
</tbody>
</table>

Elements of Transfer Diagram for an Ideal Linear DAC

Gabriel Hugh Elkaim – Fall 2014
Offset error of a Linear 3-Bit Natural Binary Code Converter (Specified at Step 000)

(a) ADC
(b) DAC
Gain Error of a Linear 3-Bit Natural Binary Code Converter (Specified at Step 111), After Correction of the Offset Error
End-Point Linearity Error of a Linear 3-Bit Natural Binary-Coded ADC or DAC (Offset Error and Gain Error are Adjusted to the Value Zero)
Differential Linearity Error of a Linear ADC or DAC
Absolute Accuracy or Total Error of a Linear ADC or DAC

(a) ADC

(b) DAC

Total Error
At Step 0...101
(± 1 1/4 LSB)

Total Error
At Step 0...001 (1/2 LSB)
Questions?
Beer Converse — Tonight

11 pm — Midnight
Announcements

Good - T-shirt in 10 days turn around
Black

Bad - Midterms are not quite done.

Ugly - we're not going to finish them today.
TX's

- Max Lichtenstein

- Marcello Guarrico
$V_{in} \quad R \quad 2R \quad \frac{1}{\frac{1}{2R}} \quad R \quad 2R \quad 2R$

$R - 2R \quad \text{ADC}$