1. (6 points) Complete the state of the NUMA control structures for the following access sequence. Time progresses first by rows.

- **Initial State**
  - CPU 0: Directory 012, X: U 000, Memory X=2, Cache
  - CPU 1: Directory, Memory, Cache
  - CPU 2: Directory, Memory, Cache

- **P1 reads X**
  - CPU 0: Directory 012, X: S 011, Memory X=2, Cache
  - CPU 1: Memory, Cache
  - CPU 2: Directory, Memory, Cache

- **P2 reads X**
  - CPU 0: Directory 012, X: S 110, Memory X=5, Cache
  - CPU 1: Memory, Cache
  - CPU 2: Directory, Memory, Cache

- **P0 reads X**
  - CPU 0: Directory 012, X: S 111, Memory X=5, Cache
  - CPU 1: Memory, Cache
  - CPU 2: Directory, Memory, Cache

- **P1 writes X**
  - CPU 0: Directory 012, X: E 010, Memory X=2 (false), Cache
  - CPU 1: Memory
  - CPU 2: Directory, Memory, Cache

- **P2 reads X**
  - CPU 0: Directory 012, X: S 111, Memory X=5, Cache
  - CPU 1: Memory
  - CPU 2: Directory, Memory, Cache

**Name:** Solutions
2. (6 points) Remember that handheld game system from the first few homeworks and quizzes? They've got a game running on it now, but it's way too slow. They want the game to run at **30 frames per second**, but currently it's taking **50ms per frame**. A quick profiling shows it spends it's time as follows:

- 40% Graphics
- 15% Sound
- 20% AI
- 20% world update
- 5% input handling

 Seeing how much time the game is spending on graphics, management tells everyone to stop what they're working on and optimize the graphics code.

a. What speedup in graphics alone would achieve the desired frame rate?

\[
\frac{20}{33.3} = \frac{600}{33} 
\]

b. Assuming that the graphics code was written by reasonably competent engineers, is this speedup likely to be achievable? Were the manager's instructions appropriate?

**No, and no.**

3. (8 points) Diagram: A virtual address, a physical address, a cache line, a TLB entry, a cache lookups, and a TLB lookup for the following memory system:

- 512MB physical address space
- 32-bit virtual address
- 32-bit physical address
- 16KB Pages
- 256-entry 2-way set-associative TLB
- 24KB 3-way set associative 1024-line cache

**Diagram:**

- Virtual Address: V.addr
  - VPN: 18
  - VPO: 14

- Physical Address: P.addr
  - PPN: 15
  - PPO: 14

- Cache Line: c.line
  - Tag: 19
  - V & other flags: 64

- TLB Entry: TLB Entry
  - Tag: 11
  - Flags: 15
  - PPN: 14

- Cache Lookup: c.lookup
  - Tag: 19
  - Index: 10
  - Offset: 14

- TLB Lookup: TLB Lookup
  - Tag: 11
  - Index: 7
  - Offset: 14