1. Traditional PCI is a “bus”. PCI-Express is not. Why?

   in “Bus” topologies, many devices are connected to the same physical wire. PCI-Express uses separate wires to connect to each device.

2. What is the theoretical peak total bidirectional bandwidth of each of the following protocols? You may need to look some of these up online.

   a. 33MHz, 64-bit PCI

      \[
      \frac{1}{3} \times 100 \times 10^6 \times 8 = 266\text{MB/s}
      \]

   b. 133MHz Quad-Pumped Dual-Channel FSB

      \[
      a = 133\text{MHz} \times \text{quad-pumped} = 533 \text{ Mtransfers/second}
      \]
      \[
      b = \text{dual-channel} = 128 \text{ bytes/transfer} = 16 \text{ bytes/transfer}
      \]
      \[
      a \times b = 8.533 \text{ GB/sec}
      \]

   c. PCIe x16

      250 MB/sec per direction per lane
      \[
      x_{16} = 16 \text{ lanes}
      \]
      4 GB/sec per direction
      8 GB/sec total

   d. 200MHZ DDR2 RAM

      200 MHz refers to bus clock, as in slides. DDR, so transfer rate is twice that (400 MHz) and width is 128 bits (8 bytes)
      \[
      400 \text{ MHz} \times 8 \text{ bytes} = 3200 \text{ MB/sec} = 3.2 \text{ GB/sec}
      \]