CMPE011 Winter 2004

Pipelined CPU

- Pipeline principles
- Pipelined datapath
- Pipelined control

Textbook: 6.1 to 6.3
Single-cycle restaurant
Multicycle restaurant
Pipelined restaurant
Pipelined datapath

What is a “pipeline”?

- just like in the multicycle datapath, there are stages
- in a pipelined architecture, however, all stages operate concurrently
- a new instruction begins execution at every clock cycle
Our multicycle datapath
Pipelined datapath
Pipeline characteristics

**number of stages:** five in the classical pipeline

(IF, ID, EX, MEM, WB — just like in the multicycle CPU)

**$T_{ck}$ limitation:** now the constraint is the longest worst-case path among all the stages

**resources:** to perform some operations concurrently, we need to duplicate some resources (like in the single-cycle implementation)
Single-cycle vs. pipeline execution
Multicycle vs. pipeline execution
Pipeline performance

**speedup:** ideal speedup = # of pipeline stages
  (only if the stages are perfectly balanced)

**CPI:** ?

**throughput:** we approach the ideal speedup only when considering the execution of many instructions

**latency time:** the execution time of a single instruction
MIPS instruction set architecture and pipelining

- all instructions are the same length
- few instruction formats (and very similar)
- memory accesses only in load/store instructions
A walk through the pipeline

With the following piece of code:

```
lw  $1 20($1)
sub $11, $2, $3
```

`lw $10, 20($1)`

`sub $11, $2, $3`
A walk through the pipeline: clock cycle 1

lw $10, 20($1)
A walk through the pipeline: clock cycle 2

sub $11, $2, $3
lw $10, 20($1)
A walk through the pipeline: clock cycle 3
A walk through the pipeline: clock cycle 4
A walk through the pipeline: clock cycle 5

sub $11, $2, $3  lw $10, 20($1)
A walk through the pipeline: clock cycle 6

sub $11, $2, $3
Pipelined control

- pipelining the datapath leaves the meaning of control lines unchanged
- control signals are pipelined too (grouped by stage)
- the control unit is combinatorial again
Pipelined control

Pipelined control: complete schematic
Recommended exercises

Ex. 6.5, 6.7, 6.9, 6.10