CMPE 100 & 100L: Introduction to Logic Design
General Information and Syllabus
Winter 2003

MWF: 12:30pm – 1:40pm
Lecture room: Social Science 2 room 071
Laboratory room: J. Baskin Engineering 104

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Important dates:
Midterm #1 is on Monday, January 27th
Midterm #2 is on Monday, February 24th
Final is on Monday, March 17th

Required Textbook:

WWW sites and Newsgroup:
Class web site:
http://www.soe.ucsc.edu/classes/cmpe100/Winter03/

Check this site regularly for announcements and handouts. It will evolve over the course of the quarter

Class Newsgroup:
ucsc.class.cmpe100

Use the newsgroup to have discussions between yourselves, the TA and tutors. If questions to the instructor are posted please also use email so a timely response can be made.

Book web site:
http://www.ddpp.com/

Text book author’s web site has lots of interesting information and some solutions and teaching aids.

Course Work:
Welcome to CMPE-100. I hope you get a lot out of this class, I feel it is one of the most interesting and fun classes available in computer engineering at UCSC.
In this course we will cover the fundamental topics necessary to successfully engineer modern logic circuit designs. This requires that we investigate two overlapping areas of study. The first gives students a firm introduction into the fundamental elements and principles of combinational (without memory) binary logic systems from a theoretical and somewhat abstract perspective. This involves: some number theory; Boolean algebra; basic logic elements; combinational logic design and programmable logic devices; hardware description languages (HDL); classic logic blocks, like decoders, multiplexers, etc. From this base we will progress to a study of finite state machines or digital systems that involve memory. This topic includes: flip-flops of all types, clocks, synchronous and asynchronous state machines.

The second area of study deals with how to actually build or implement logic designs. Here we investigate particular logic device families and their unique electrical characteristics. Typically, this will include: classic TTL, CMOS and other discrete logic families, familiarization with laboratory equipment to observe, measure and appreciate how voltage is used to represent abstract binary states including basic time-domain depictions via timing diagrams. Since this area draws upon properties of basic electrical circuits, EE-70 is recommended but not required.

You will be given weekly homework assignments. I strongly suggest you take them seriously as they will prepare you for the exams and keep you in synch with the lectures as we will build upon material over the entire quarter. You should try to do the assignments first independently before consulting other students for aid. Appropriate aid is a TA/Tutor/friend showing you how to do the problem, not doing the problem for you. You are not allowed at anytime to simply copy someone else’s assignment. If collaboration was done you must put the person’s name on your assignment.

Academic honesty is a requirement for the course. Cheating on the midterms or final will result in failure in the course (class and lab) and you will be reported to your college and your department.

If you have any disability-related needs, be sure to contact the Disability Resource Center and the instructor well in advance of any expected need.

Evaluation:

The evaluation criteria for CE100 will be homework assignments (20%), midterm #1 (20%), midterm #2 (20%) and a comprehensive final (40%).

Labwork:

You are required to keep a proper chronologically ordered engineering notebook that will be used along with your lab demonstrations as the evaluation criteria for CE100L. The notebook will contain your complete lab report write-up plus all engineering notes. More information on this will be covered in class.

Unlimited and unsupervised use of the laboratory equipment (computers, printers, etc) and resources (web access, email, ftp, etc) is a privilege, not a right. Any abuse of equipment or misuse of resources will result in the immediate loss of these privileges, and may result in disciplinary action by the University. Police this space at all times as one student’s bad behavior could result in the entire class losing their privileges to the laboratory. You will be spending a lot of time in this space so help keep it clean. At no time should you bring food or drink in the lab; take coffee/snake breaks.

You will be allowed to work with a partner and discussions between groups are allowed though sharing of work is not. You are expected to keep your own notebook and are required to be able to demo and explain the entire lab assignment with out aid of your partner.