Delay is due to propagation delay of gates:

- time for the output to respond to an input change

\[ t_{phl} \quad t_{plh} \]

may be different for high $\rightarrow$ low and low $\rightarrow$ high transitions.
... and wire delays:

- Fanout
- Capacitance
- Resistance
Glitches result from logic paths with different propagation delays

```
0  |  x  |
   |     |
   |  A  |
   |     |
   |  C  |
   |     |
   |  D  |
```

```
X
A
B
C
D
```
... or merely from wiring delays:

1 $Q_3$
0 $Q_2$
0 $Q_1$
0 $Q_0$

TC

Remember Lab 1 →
Glitches are not a problem on *synchronous signals* (Signals used only by components with same clock)

Signals need only be correct and stable near the clock edge.

Clock period needs to be longer than the largest logic delay.
Static Timing Analysis: Critical path

Arrival time of input = Delay of source gate + wire delay

Delay of gate output = gate delay + arrival time of latest input
Static Timing Analysis: Critical path

Assume:
- Each gate has a propagation delay of 2
- Wire delays are as labeled.

Critical paths are the longest input-to-output paths.

Starting from latest output trace backwards following the latest arriving inputs.
clock period must be longer than the largest FF to FF delay