module control_logic(wheel, timeUp, PS, NS, reset_timer, bike);
    input wheel;
    input timeUp;
    input [4:0] PS;
    output [4:0] NS;
    output reset_timer;
    output bike;
    wire   IDLE, FW, BTW, RW, ERROR;
    wire   Next_IDLE, Next_FW, Next_BTW, Next_RW, Next_ERROR;
    assign IDLE  = PS[0];
    assign FW    = PS[1];
    assign BTW   = PS[2];
    assign RW    = PS[3];
    assign ERROR = PS[4];
    assign NS[0] = Next_IDLE;
    assign NS[1] = Next_FW;
    assign NS[2] = Next_BTW;
    assign NS[3] = Next_RW;
    assign NS[4] = Next_ERROR;
    assign Next_IDLE  = IDLE&~wheel | RW&~wheel;
    assign Next_FW    = (IDLE|ERROR)&wheel | FW&wheel;
    assign Next_BTW   = BTW&~wheel&~timeUp | FW&~wheel;
    assign Next_RW    = RW&wheel | BTW&wheel;
    assign Next_ERROR = ERROR&~wheel | BTW&timeUp&~wheel;
    assign bike        = RW&~wheel;
    assign reset_timer = FW&~wheel;
endmodule