Introduction to Logic Design  
General Information and Syllabus

Days/Times: MWF: 11:00am – 12:10pm  
Lecture room: Kresge Classroom 327  
Laboratory room: J. Baskin Engineering 104

Instructor: Cyrus Bazeghi  
E-mail: cyrus@cse.ucsc.edu  
Office: ISB 111 (next to the Science and Engineering Library)  
Office Hours: 1pm – 2pm MWF and by appointment  
Home: (831) 465-0582  
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TA’s: Graham Brown (monchee@cse.ucsc.edu)  
Yue Zhou (zhou@soe.ucsc.edu)

Lab Tutors (so far):  
Jon Webb (jonwebb@cats.ucsc.edu)  
Adam Harrison (adam@cats.ucsc.edu)  
Eric Cain (ecain@phosphor.net)  
Michael Fahmie (pengo@cats.ucsc.edu)

Important dates

Midterm is on Friday, May 3rd, 11:00 am – 12:10 pm  
Final is on Thursday, June 6th, 12:00 – 3:00 pm

Textbook:


WWW sites:

Class web site:  
http://www.soe.ucsc.edu/classes/cmpe100/Spring02/  
Check this site regularly for announcements and handouts. It will evolve over the course of the quarter  
Book web site:  
http://www.ddpp.com/  
Text book author’s web site, has lots of interesting information and some solutions and teaching aids.

Course Work: (some excerpts from Stephen Petersen’s course description, Winter 2002)

Welcome to CMPE-100, I hope you get a lot out of this class, I feel it is one of the most interesting and fun classes available in computer engineering at UCSC.

In this course we will cover the fundamental topics necessary to successfully engineer modern logic circuit designs. This requires that we investigate two overlapping areas of study. The first gives students
a firm introduction into the fundamental elements and principles of combinational (without memory) binary logic systems from a theoretical and somewhat abstract perspective. This involves: some number theory; Boolean algebra; basic logic elements; combinational logic design and programmable logic devices; hardware description languages (HDL); classic logic blocks, like decoders, multiplexers, etc. From this base we will progress to a study of finite state machines or digital systems that involve memory. This topic includes: flip-flops or all types, clocks, synchronous and asynchronous state machines.

The second area of study deals with how to actually build or implement logic designs. Here we investigate particular logic device families and their unique electrical characteristics. Typically, this will include: classic TTL, CMOS and other discrete logic families; familiarization with laboratory equipment to observe, measure and appreciate how voltage is used to represent abstract binary states including basic time-domain depictions via timing diagrams. Since this area draws upon properties of basic electrical circuits, EE-70 is recommended but not required.

You will be given weekly homework assignments. I strongly suggest you take them seriously as they will prepare you for the exams and keep you in synch with the lecturers as we will build upon things. You should try to do the assignments first independently before consulting other students.

Academic honesty is a requirement for the course. Cheating on the midterm or final will result in failure in the course and you will be reported to your college and your department.

If you have any disability-related needs, be sure to contact the Disability Resource Center well in advance of any expected need.

Evaluation:

The evaluation criteria for CE100 will be homework assignments (25%), a midterm (35%), and a final (40%).

Labwork:

You are required to keep a proper chronologically ordered engineering notebook that will be used along with your lab demonstrations as the evaluation criteria for CE100L. There is no required form for this notebook, it can be bound or spiral, it just needs to have pages numbered and in a neat and chronological order.

Unlimited and unsupervised use of the laboratory equipment (computers, printers, etc) and resources (web access, email, ftp, etc) is a privilege not a right. Any abuse of equipment or misuse of resources will result in the immediate loss of these privileges, and may result in disciplinary action by the University. Police this space at all times as one student’s bad behavior could result in the entire class losing their privileges to the laboratory.

NOTE: ALL FOOD AND BEVERAGES ARE EXPRESSLY PROHIBITED IN THE LAB AND THE DOOR SHOULD NEVER BE LEFT PROPPED OPEN.