Delay is due to propagation delay of gates:

time for the output to respond to an input change

may be different for high low and low high transitions

... and wire delays:

- Fanout
- Capacitance
- Resistance

Glashes result from logic paths with different propagation delays

... or merely from wiring delays:

Remember Lab 1
Glitches are not a problem on synchronous signals
(Signals used only by components with same clock)

Signals need only be correct and stable near the clock edge.

Clock period needs to be longer than the largest logic delay.

Static Timing Analysis: Critical path

Assume:
Each gate has a propagation delay of 2
Wire delays are as labeled.

Clock period must be longer than the largest FF to FF delay