Field Programmable Gate Arrays

Large number of interconnected programmable logic blocks. Some are connected to I/O pads as well.

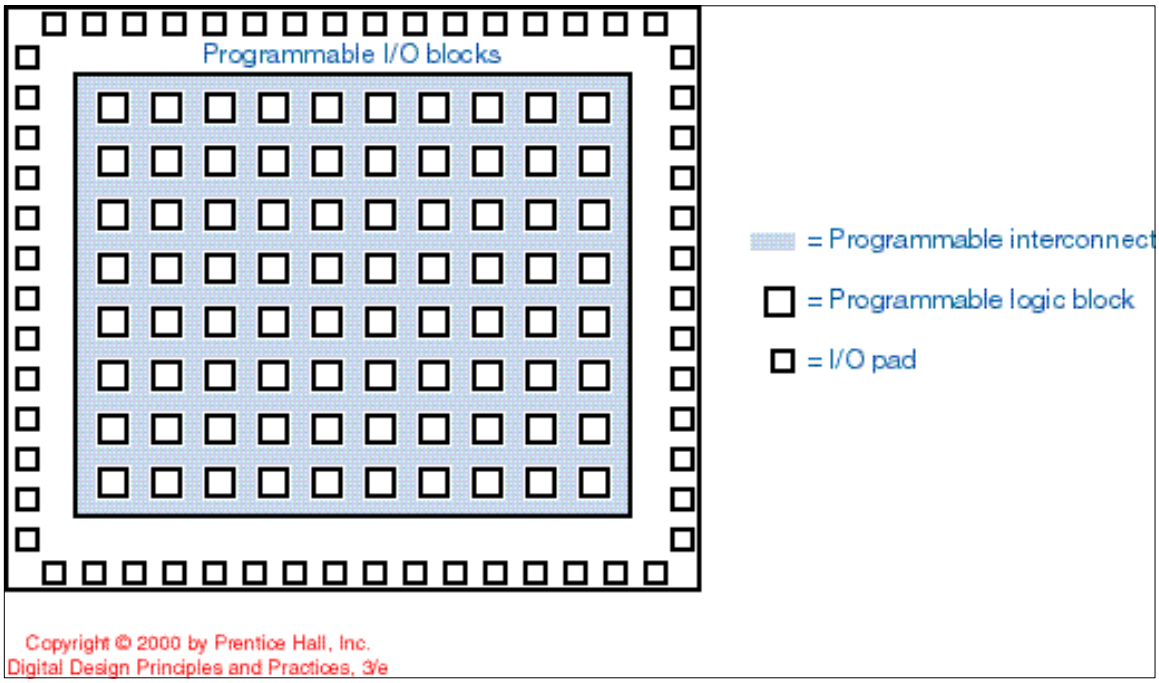
Xilinx calls the Programmable Logic Blocks – Configurable Logic Blocks (CLBs)

FPGAs can be summarized in one word

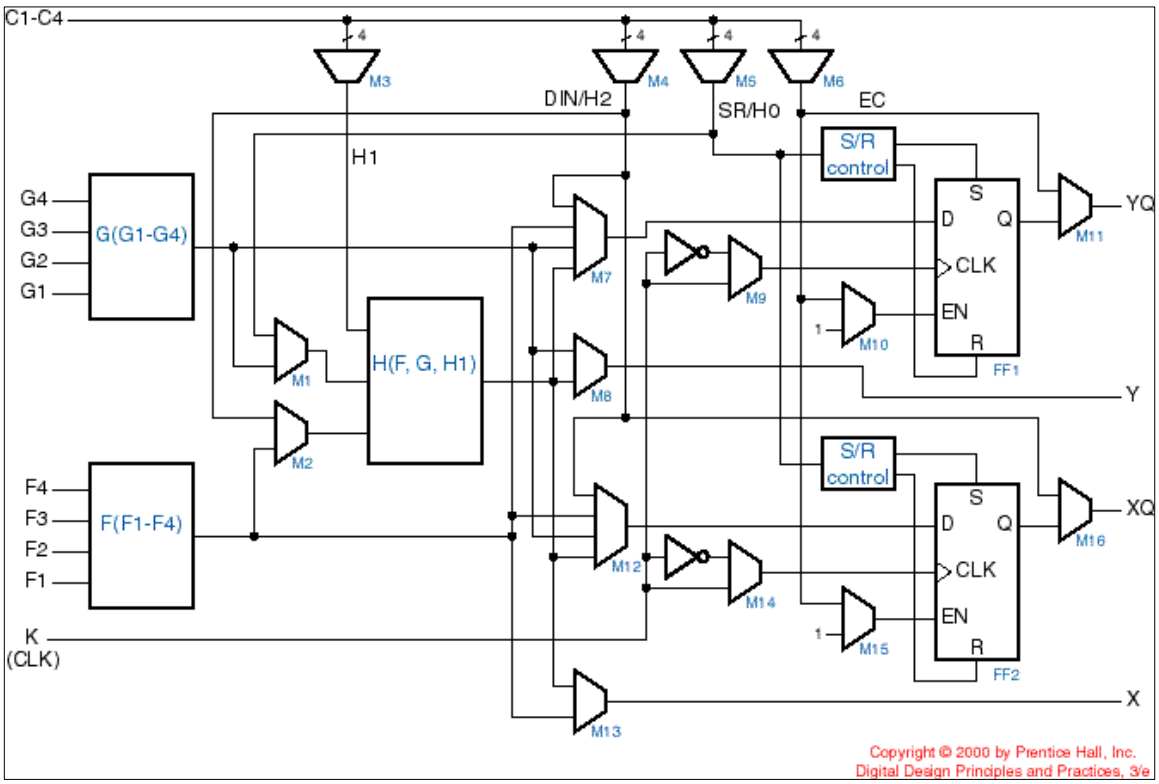
___LUT____

(LOOK UP TABLE)

A typical layout of the FPGA is an array of interconnected programmable logic blocks or configurable logic blocks. The logic blocks are sitting in a "sea" of interconnect wires. Interconnects between wires are programmed by turning on/off transistors at the wire junctions similar to how programmable array logic (PLD) works (using a floating gate CMOS transistor). Large numbers of PLB or CLBs can be wired together using this technique. Input/output from the FPGA is handled via special I/O pads which themselves also contain sequential logic circuitry.



FPGA - Configurable Logic Block - XC4000 Series CLB



Logic Function Generators (G, F, H)

F & G- 4- input (16 x 1 SRAM)
A function of 4 variables input can be realized with a truth table. That table is stored in the F & G "Function Generators"

H – 3 input (8 x 1 SRAM)
A function of 3 variables input, realized by table is stored in the H "Function Generators".

Functions that can be realized using F,G & H together.

- *Any function of 4-inputs, plus any 2nd function of 4 unrelated inputs, plus a 3rd function of 3 unrelated inputs*
- *A single function of 5 variables.*
- *Any function of 4 variable, plus some 2nd function of 6 unrelated variables.*
- *Some functions up to 9-input variables.*

Input/Output PADS

Shown below is the I/O pad block. D-flops are used to hold outgoing and incoming data. Most of the remainder of circuit are multiplers to choose value or its complement. Finally at the output pin itself, there is a transistor network to supply/sink current for driving devices outside (fanout related).