CMPE100, Fall 2002
Final Exam Parameters

Exam will be comprehensive but emphasize material covered since Ch 4.
Based on quizzes, assigned homework, supporting sections from the textbook and material
introduced in lecture.

The exam will be closed-book. **Bring a working calculator**!
Any necessary datasheets or figures will be available as part of the exam.

CMPE100 Catalog Description

*Must be familiar with and be able to reason about discrete logic with an introduction to Boolean
logic. They must be able to manipulate logic expressions, understand truth tables and be very
familiar with deMorgan’s laws.*

Upon Successful completion of course, student is expected to have the following skill elements:

<table>
<thead>
<tr>
<th>Element</th>
<th>Skill</th>
<th>Exam Section</th>
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<tbody>
<tr>
<td>1</td>
<td>Minimize logic using Boolean Algebra (taught in CMPE16)</td>
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<tr>
<td>2</td>
<td>Minimize 2-level logic using Karaugh Maps.</td>
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<td>3</td>
<td>Use elementary logic blocks such as multiplexers, decoders and flip-flops.</td>
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<td>4</td>
<td>Translate a problem description to a state table, state diagram.</td>
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<td>5</td>
<td>Realize a finite state machine from a state table or state diagram using elementary gates and D flip-flops.</td>
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<tr>
<td>6</td>
<td>Read &amp; draw schematic diagrams of logic circuits fluently with good understanding of the inverter-bubble convention.</td>
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<tr>
<td>7</td>
<td>Read timing diagrams.</td>
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<td>8</td>
<td>Understand concepts of propagation delay and fanout, including crude RC timing models for CMOS and the importance of capacitive loading.</td>
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<tr>
<td>9</td>
<td>Understand CMOS logic circuits at the switch level.</td>
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What will be on Final….

*Most emphasis on:*
- A simple state machine design problem. Translate a word description to state table and/or state diagram.
- Derive excitation equations from a state table or state diagram and realize the finite state machine (will provide function table for JK).
- Feedback sequential machine analysis. Understand and identify races.

*In addition, the following areas are strong candidates for questions.*
- Questions frequently missed on the quizzes are strong candidates for inclusion on the Final.
- Be able to apply DeMorgan’s theorem to help solve some problems. Remember “push the bubble through” technique.
- K-map logic minimization, POS, SOP, XOR (checkerboard patterns).
- Timing Diagram Problem; both for combinational logic and sequential logic. *If setup & hold times are given in a problem you should assume they may be needed. Otherwise assume they are very small.*
- A problem involving decoders/multiplexers to implement combinational logic.
- Some basic questions on FPGAs & how they work *(not on any past quiz)*
- CMOS logic structures (NAND, NOR, INVERTER).
- RC Time constant. Determine value, indicate what happens to rise & fall times but not calculating them (rise/fall times).
- Propagation delay through a multi-level circuit.
- A problem with Fanout and circuit interfacing (e.g. HC, LS, HCT).
- Hazards and glitches, what causes them and how eliminate them by covering the hazard.
- Static-0 and static-1 hazards. What are they?

Minor problems on the following. Questions here will typically be multiple choice or short answer.

- Number system conversions (hex, decimal, binary)
- 2’s complement addition & subtraction
- Gray code
- Complex programmable logic devices. You should know how these devices were related to earlier PLD’s and the differences between them and FPGAs.
- Field programmable logic arrays (FPGAs; 10.6). The same comments as those noted for CPLDs apply here. Relevant figures from the text are: Fig. 10-43 to 48. You should also know what the various columns in Table 10-9 mean.