1) (2 pts) Trace the instruction ‘addi $s0, $s1, 0x23’ through the architecture.

2) (2 pts) Trace the instruction ‘add $s0, $s1, $s2’ through the architecture.
3) (2 pts) Trace the instruction ‘bgez $s0, Immed’ through the architecture.

![Diagram of instruction flow](image)

**Figure 3.1** The implementation of the DLX datapath allows every instruction to be executed in four or five clock cycles.

4) (4 pts) What is the difference between a Trap and an Interrupt in terms of:
   
   a. Nature (what causes each?)
   
   b. Function (how is each used/what problem does each solve?)