\[ 0 \bigg| \begin{array}{c} -1 \end{array} \bigg] \begin{array}{c} \text{odd} \\ \text{even} \end{array} \]
Midterm Date: February 16th, 
Review on Friday the 12th, 5PM hopefully 
Homework: base 3 not base -3. Turn it in either way for credit 
Late Day form on Ecommons, please fill out for assignments already turned in

assigned seating
LC-3 Architecture

(Ch4’ish material)
CISC vs. RISC

CISC: Complex Instruction Set Computer
Lots of instructions of variable size, very memory optimal, typically less registers.

RISC: Reduced Instruction Set Computer
Less instructions, all of a fixed size, more registers, optimized for speed. Usually called a “Load/Store” architecture.
What is “Modern”

For embedded applications and for workstations there exist a wide variety of CISC and RISC and CISCy RISC and RISCy CISC.

Most current PCs use the best of both worlds to achieve optimal performance.
LC-3 Architecture

- Very RISC, only 15 instructions
- 16-bit data and address
- 8 general purpose registers (GPR)
- Program Counter (PC)
- Instruction Register (IR)
- Condition Code Register (CC)
- Process Status Register (PSR)
Instruction Fetch / Execute Cycle

In addition to input & output a program also:

- Evaluates arithmetic & logical functions to determine values to assign to variable.
- Determines the order of execution of the statements in the program.

In assembly this distinction is captured in the notion of **Arithmetic, logical, and control** instructions.
Instruction Fetch / Execute Cycle

\[ a = b + c \]

**Arithmetic** and **logical** instructions evaluate variables and assign new values to variables.

**Control instructions** test or compare values of a variable and makes decisions about what instruction is to be executed next.

**Program Counter (PC)**
Basically the address at which the current executing instruction exists, or the next instruction.
Instruction Fetch / Execute Cycle

\[ c = a + b \]

1. load rega, 10
2. load regb, 20
3. add regc, rega, regb
4. beq regc, regd, 8
5. store regd, rege
6. store regc, regd
7. load regb, 15
8. load rega, 30

*Note: This is just pseudo assembly code*
Instruction Fetch / Execute Cycle

\[ a = b + c \rightarrow PC \]
\[ c = 2 \cdot a \, \checkmark \]

The CPU begins the execution of an instruction by supplying the value of the PC to the memory & initiating a read operation (fetch).

The CPU “decodes” the instruction by identifying the opcode and the operands.

PC increments automatically unless a control instruction is used.
Instruction Fetch / Execute Cycle

For example:

PC → ADD A, B, C

- CPU fetches instruction
- Decodes it and sees it is an “add” operation, needs to get values for the variables “B” & “C”
- Gets the variable “B” from a register or memory
- Does the same for variable “C”
- Does the “add” operation and stores the result in location register for variable “A”

\[ a = b + c + d \]
Instruction Fetch / Execute Cycle

**Branch** – like a goto instruction, next instruction to be fetched & executed is an instruction other than the next in memory.

```
ADD A, B, C
BRn fred
ADD A, D, 3
ADD A, D, 4
```

If A is negative then next instruction to be executed is at “fred”, which is just an address

*Note: This is almost real LC-3 assembly*
Breaking down an instruction

MAL has an 8-bit opcode. Variables a, b, and c each require an address to specify their memory location. If addresses are 32-bit then this is 104 bits, not a 32-bit instruction. How?

Memory accesses take more time than arithmetic and logical operations. Why? No memory fetches from slow, external parts. If we have a 32-bit memory interface this operation would take 7 memory accesses. 4 to fetch the instruction (104 bits), one for each of the operands B and C and one more to store the result C.

\[
ADD \ a, \ b, \ c
\]

\[
\begin{array}{c|c|c|c|c}
\text{add} & a & b & c \\
\end{array}
\]

\[
\text{Opcode}
\]

\[
\text{Destination register}
\]

\[
\text{Source registers/immediate}
\]

\[
a = b + c
\]

\[
a = 5
\]
The Stored Program Computer

1943: ENIAC
- Presper Eckert and John Mauchly -- first general electronic computer. (or was it John V. Atanasoff in 1939?)
- Hard-wired program -- settings of dials and switches.

1944: Beginnings of EDVAC
- among other improvements, includes program stored in memory

1945: John von Neumann
- wrote a report on the stored program concept, known as the First Draft of a Report on EDVAC
First Draft of a Report on EDVAC

The basic structure proposed in the draft became known as the “von Neumann machine” (or model).

This machine/model had five main components:

– a memory, containing instructions and data
– a processing unit, for performing arithmetic and logical operations
– a control unit, for interpreting instructions
– and input and output to get data into and out of the system.
Von Neumann Model*

* A slightly modified version of Von Neumann’s original diagram
Locality of reference

We need techniques to reduce the instruction size. From observation of programs we see that a small and predictable set of variables tend to be referenced much more often than other variables.

Basically, locality is an indication that memory is not referenced randomly.

This is where the use of registers comes into play.
Memory

$2^k \times m$ array of stored bits:

- **Address**
  - unique ($k$-bit) identifier of location
- **Contents**
  - $m$-bit value stored in location

**Basic Operations:**

- **LOAD**
  - read a value from a memory location
- **STORE**
  - write a value to a memory location
Interface to Memory

How does the processing unit get data to/from memory?

**MAR**: Memory Address Register

**MDR**: Memory Data Register

To **LOAD** a location (A):

1. Write the address (A) into the MAR.
2. Send a “read” signal to the memory.
3. Read the data from MDR.

To **STORE** a value (X) to a location (A):

1. Write the data (X) to the MDR.
2. Write the address (A) into the MAR.
3. Send a “write” signal to the memory.
<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
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<tr>
<td>0</td>
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<td>1</td>
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<td>1</td>
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<td>1</td>
</tr>
</tbody>
</table>

\[ \overline{D} \text{ and } WE \]
\[ D \text{ and } WE \quad 0 \]

\[ \overline{WE} \]
Von Neumann Model

Processing Unit

Functional Units
- ALU = Arithmetic and Logic Unit
- could have many functional units. some of them special-purpose (multiply, square root, ...)
- LC-3 performs ADD, AND, NOT

Registers
- Small, temporary storage
- Operands and results of functional units
- LC-3 has eight registers (R0, ..., R7), each 16 bits wide

Word Size
- number of bits normally processed by ALU in one instruction
- also width of registers
- LC-3 is 16 bits
Input and Output

Devices for getting data into and out of computer memory

Each device has its own interface, usually a set of registers like the memory’s MAR and MDR

- LC-3 supports keyboard (input) and monitor (output)
- keyboard: data register (KBDR) and status register (KBSR)
- monitor: data register (DDR) and status register (DSR)

Some devices provide both input and output
- disk, network

The program that controls access to a device is usually called a driver.
Control Unit

Controls the execution of the program

**Instruction Register** (IR) contains the *current instruction*.

**Program Counter** (PC) contains the *address* of the next instruction to be executed.

**Control unit:**
- reads an instruction from memory
  - the instruction’s address is in the PC
- interprets the instruction, generating signals that tell the other components what to do
  - an instruction may take many *machine cycles* to complete
Instructions

The instruction is the fundamental unit of work. Specifies two things:

- *opcode*: operation to be performed
- *operands*: data/locations to be used for operation
An instruction is encoded as a sequence of bits. *(Like data)*

- Often, but not always, instructions have a fixed length, such as 16 or 32 bits. *(RISC vs. CISC)*
- Control unit interprets instruction: generates sequence of control signals to carry out operation.
- Operation is either executed completely, or not at all.

A computer’s instructions and their formats is known as its *Instruction Set Architecture (ISA)*.
Ex: LC-3 ADD Instruction

LC-3 has 16-bit instructions.

- Each instruction has a four-bit opcode, bits [15:12].

LC-3 has 8 registers (R0-R7) for temp. storage.

- Sources and destination of ADD are registers.

```
   15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
  ADD  Dst  Src1  0 0 0  Src2
```

```
   15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
0 0 0 1 1 1 0 0 1 0 0 0 0 0 1 1 0
```

“Add the contents of R2 to the contents of R6, and store the result in R6.”
Ex: LC-3 LDR Instruction

Load instruction -- reads data from memory

Base + offset mode:
- add offset to base register - result is memory address
- load from memory address into destination register

```
 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
```
```
  LDR  Dst  Base  Offset
```
```
 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
```
```
 0 1 1 0 0 1 0 0 1 1 0 0 0 0 1 1 0
```

“Add the value 6 to the contents of R3 to form a memory address. Load the contents of that memory location to R2.”
Instruction Processing

1. Fetch instruction from memory
2. Decode instruction
3. Evaluate address
4. Fetch operands from memory
5. Execute operation
6. Store result
FETCH

Load next instruction (at address stored in PC) from memory into Instruction Register (IR).
- Copy contents of PC into MAR.
- Send “read” signal to memory.
- Copy contents of MDR into IR.

Then increment PC, so that it points to the next instruction in sequence.
- PC becomes PC+1.
First identify the opcode.
- In LC-3, this is always the first four bits of instruction.
- A 4-to-16 decoder asserts a control line corresponding to the desired opcode.

Depending on opcode, identify other operands from the remaining bits.
- Example:
  - for LDR, last six bits is offset
  - for ADD, last three bits is source operand #2
EVALUATE ADDRESS

For instructions that require memory access, compute address used for access.

Examples:
- add offset to base register (as in LDR)
- add offset to PC
- add offset to zero
FETCH OPERANDS

Obtain source operands needed to perform operation.

Examples:
- load data from memory (LDR)
- read data from register file (ADD)
EXECUTE

Perform the operation, using the source operands.

Examples:
- send operands to ALU and assert ADD signal
- do nothing (e.g., for loads and stores)
Write results to destination. (register or memory)

Examples:
- result of ADD is placed in destination register
- result of memory load is placed in destination register
- for store instruction, data is stored to memory
  - write address to MAR, data to MDR
  - assert WRITE signal to memory
Changing the Sequence of Instructions

In the FETCH phase, we increment the Program Counter by 1.

What if we don’t want to always execute the instruction that follows this one?
- examples: loop, if-then, function call
We need special instructions that change the contents of the PC.

These are those control instructions from before.

- **jumps** are unconditional -- they always change the PC
- **branches** are conditional -- they change the PC only if some condition is true (e.g., the result of an ADD is zero)
Ex: LC-3 JMP

Set the PC to the value contained in a register. This becomes the address of the next instruction to fetch.

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
| JMP | 0 0 0 | Base | 0 0 0 0 0 0 0 |
```

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
| 1 1 0 0 0 0 0 0 | 0 1 1 | 0 0 0 0 0 0 0 |
```

“Load the contents of R3 into the PC.”
Instruction Processing

Summary

Instructions look just like data -- it’s all interpretation.

Three basic kinds of instructions:
- computational instructions (ADD, AND, ...)
- data movement instructions (LD, ST, ...)
- control instructions (JMP, BRnz, ...)
Six basic phases of instruction processing:

F $\rightarrow$ D $\rightarrow$ EA $\rightarrow$ OP $\rightarrow$ EX $\rightarrow$ S

- Not all phases are needed by every instruction
- Phases may take more than 1 machine cycle
2's complement

\[-2\]
\[-3\]
\[-2 + -3\]

\[-2\]
\[-3\]
\[-2 + -3\]

\[\frac{-2}{-3}\]
\[-2 + -3\]

\[\frac{2}{-3}\]
\[-3\]

\[-(3 - 2)\]
2 - 3 in 2's complement

2 + (-3)

0011

1100

+ 1

1101

0010

+ 11101

11111