ADD R1, R1, 4

LC-3 Architecture

(Ch4’ish material)
LC-3 Architecture

- Very RISC, only 15 instructions
- 16-bit data and address
- 8 general purpose registers (GPR)
- Program Counter (PC)
- Instruction Register (IR)
- Condition Code Register (CC)
- Process Status Register (PSR)
Instruction Fetch / Execute Cycle

In addition to input & output a program also:

- Evaluates arithmetic & logical functions to determine values to assign to variable.
- Determines the order of execution of the statements in the program.

In assembly this distinction is captured in the notion of **Arithmetic**, **logical**, and **control** instructions.
Instruction Fetch / Execute Cycle

**Arithmetic** and **logical** instructions evaluate variables and assign new values to variables.

**Control instructions** test or compare values of a variable and makes decisions about what instruction is to be executed next.

**Program Counter (PC)**
Basically the address at which the current executing instruction exists, or the next instruction.
Instruction Fetch / Execute Cycle

1. load rega, 10
2. load regb, 20
3. add regc, rega, regb
4. beq regc, regd, 8
5. store regd, rege
6. store regc, regd
7. load regb, 15
8. load rega, 30

*Note: This is just pseudo assembly code
Instruction Fetch / Execute Cycle

The CPU begins the execution of an instruction by supplying the value of the PC to the memory & initiating a read operation (fetch).

The CPU “decodes” the instruction by identifying the opcode and the operands.

PC increments automatically unless a control instruction is used.
Instruction Fetch / Execute Cycle

For example:

PC → ADD A, B, C

- CPU fetches instruction
- Decodes it and sees it is an “add” operation, needs to get values for the variables “B” & “C”
- Gets the variable “B” from a register or memory
- Does the same for variable “C”
- Does the “add” operation and stores the result in location register for variable “A”
Instruction Fetch / Execute Cycle

**Branch** – like a goto instruction, next instruction to be fetched & executed is an instruction other than the next one in memory.

If A is negative then next instruction to be executed is at “fred”, which is just an address.

*Note: This is almost real LC-3 assembly*
The Stored Program Computer

1943: ENIAC
- Presper Eckert and John Mauchly -- first general electronic computer. (or was it John V. Atanasoff in 1939?)
- Hard-wired program -- settings of dials and switches.

1944: Beginnings of EDVAC
- among other improvements, includes program stored in memory

1945: John von Neumann
- wrote a report on the stored program concept, known as the First Draft of a Report on EDVAC
First Draft of a Report on EDVAC

The basic structure proposed in the draft became known as the “von Neumann machine” (or model).

This machine/model had five main components:

- a memory, containing instructions and data
- a processing unit, for performing arithmetic and logical operations
- a control unit, for interpreting instructions
- and input and output to get data into and out of the system.
Von Neumann Model*

* A slightly modified version of Von Neumann’s original diagram
Locality of reference

We need techniques to reduce the instruction size. From observation of programs we see that a small and predictable set of variables tend to be referenced much more often than other variables.

Basically, locality is an indication that memory is not referenced randomly.

This is where the use of registers comes into play.
Memory

$2^k \times m$ array of stored bits:

- Address
  - unique ($k$-bit) identifier of location
- Contents
  - $m$-bit value stored in location

Basic Operations:

- **LOAD**
  - read a value from a memory location
- **STORE**
  - write a value to a memory location
Interface to Memory

How does the processing unit get data to/from memory?

MAR: Memory Address Register
MDR: Memory Data Register

To **LOAD** a location (A):
1. Write the address (A) into the MAR.
2. Send a “read” signal to the memory. [wait ?]
3. Read the data from MDR.

To **STORE** a value (X) to a location (A):
1. Write the data (X) to the MDR.
2. Write the address (A) into the MAR.
3. Send a “write” signal to the memory.
Von Neumann Model

Processing Unit

Functional Units
- ALU = Arithmetic and Logic Unit
- could have many functional units, some of them special-purpose (multiply, square root, ...)
- LC-3 performs ADD, AND, NOT

Registers
- Small, temporary storage
- Operands and results of functional units
- LC-3 has eight registers (R0, ..., R7), each 16 bits wide

Word Size
- number of bits normally processed by ALU in one instruction
- also width of registers
- LC-3 is 16 bits
Input and Output

Devices for getting data into and out of computer memory

Each device has its own interface, usually a set of registers like the memory’s MAR and MDR

- LC-3 supports keyboard (input) and monitor (output)
- keyboard: data register (KBDR) and status register (KBSR)
- monitor: data register (DDR) and status register (DSR)

Some devices provide both input and output
- disk, network

The program that controls access to a device is usually called a driver.
Control Unit

Controls the execution of the program

**Instruction Register (IR)** contains the **current instruction**.

**Program Counter (PC)** contains the **address** of the next instruction to be executed.

**Control unit:**
- reads an instruction from memory
  - the instruction’s address is in the PC
- interprets the instruction, generating signals that tell the other components what to do
  - an instruction may take many **machine cycles** to complete
Instructions

The instruction is the fundamental unit of work.
Specify two things:

- **opcode**: operation to be performed
- **operands**: data/locations to be used for operation
An instruction is encoded as a sequence of bits. (Like data)

- Often, but not always, instructions have a fixed length, such as 16 or 32 bits. (RISC vs. CISC)
- Control unit interprets instruction: generates sequence of control signals to carry out operation.
- Operation is either executed completely, or not at all.

A computer’s instructions and their formats is known as its Instruction Set Architecture (ISA).
Ex: LC-3 ADD Instruction

LC-3 has 16-bit instructions.
- Each instruction has a four-bit opcode, bits [15:12].
LC-3 has 8 registers (R0-R7) for temp. storage.
- Sources and destination of ADD are registers.

```
<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADD</td>
<td>Dst</td>
<td>Src1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

```
<table>
<thead>
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<th>15</th>
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<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
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<th>1</th>
<th>0</th>
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</thead>
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<td>0</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>110</td>
<td>010</td>
<td>000</td>
<td>000</td>
<td>011</td>
<td>110</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

“Add the contents of R2 to the contents of R6, and store the result in R6.”

Maxwell James Dunne
Ex: LC-3 LDR Instruction

Load instruction -- reads data from memory

Base + offset mode:

- add offset to base register - result is memory address
- load from memory address into destination register

```
  | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
  +---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
LDR |   | Dst|   | Base|   |   | Offset |
```

```
  | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
  +---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
0110 | 0110 | 0110 | 00001110 |
```

“Add the value 6 to the contents of R3 to form a memory address. Load the contents of that memory location to R2.”
Instruction Processing

1. Fetch instruction from memory
2. Decode instruction
3. Evaluate address
4. Fetch operands from memory
5. Execute operation
6. Store result
Instruction Processing

**FETCH**

Load next instruction (at address stored in PC) from memory into Instruction Register (IR).

- Copy contents of PC into MAR.
- Send “read” signal to memory.
- Copy contents of MDR into IR.

Then increment PC, so that it points to the next instruction in sequence.

- PC becomes PC+1.
First identify the opcode.
  - In LC-3, this is always the first four bits of instruction.
  - A 4-to-16 decoder asserts a control line corresponding to the desired opcode.

Depending on opcode, identify other operands from the remaining bits.
  - Example:
    - for LDR, last six bits is offset
    - for ADD, last three bits is source operand #2
EVALUATE ADDRESS

For instructions that require memory access, compute address used for access.

Examples:
- add offset to base register (as in LDR)
- add offset to PC
- add offset to zero

TRAP
FETCH OPERANDS

Obtain source operands needed to perform operation.

Examples:
- load data from memory (LDR)
- read data from register file (ADD)
EXECUTE

Perform the operation, using the source operands.

Examples:
- send operands to ALU and assert ADD signal
- do nothing (e.g., for loads and stores)
Write results to destination.
(register or memory)

Examples:
- result of ADD is placed in destination register
- result of memory load is placed in destination register
- for store instruction, data is stored to memory
  - write address to MAR, data to MDR
  - assert WRITE signal to memory
Changing the Sequence of Instructions

In the FETCH phase, we increment the Program Counter by 1.

What if we don’t want to always execute the instruction that follows this one?
– examples: loop, if-then, function call
Changing the Sequence of Instructions

We need special instructions that change the contents of the PC.

These are those control instructions from before.

- **jumps** are unconditional -- they always change the PC
- **branches** are conditional -- they change the PC only if some condition is true (e.g., the result of an ADD is zero)
Ex: LC-3 JMP

Set the PC to the value contained in a register. This becomes the address of the next instruction to fetch.

```
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

| JMP | 0 0 0 | Base | 0 0 0 0 0 0 0 |
```

```
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

1 1 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0
```

“Load the contents of R3 into the PC.”
Instruction Processing
Summary

Instructions look just like data -- it’s all interpretation.

Three basic kinds of instructions:
– computational instructions (ADD, AND, ...)
– data movement instructions (LD, ST, ...)
– control instructions (JMP, BRnz, ...)
Six basic phases of instruction processing:

\[ F \rightarrow D \rightarrow EA \rightarrow OP \rightarrow EX \rightarrow S \]

- Not all phases are needed by every instruction
- Phases may take more than 1 machine cycle
LC-3
Instruction Set Architecture
(Ch5)
Instruction Set Architecture

ISA is all of the *programmer-visible* components and operations of the computer.

- memory organization
  - address space -- how many locations can be addressed?
  - addressability -- how many bits per location?
- register set
  - how many? what size? how are they used?
- instruction set
  - opcodes
  - data types
  - addressing modes

The ISA provides all the information needed for someone to write a program in machine language (or translate from a high-level language to machine language).
Memory vs. Registers

Memory
- address space: $2^{16}$ locations (16-bit addresses)
- addressability: 16 bits

Registers
- temporary storage, accessed in a single machine cycle
  - accessing memory generally takes longer than a single cycle
- eight general-purpose registers: R0 - R7
  - each is 16 bits wide
  - how many bits to uniquely identify a register?
- other registers
  - not directly addressable, but used/effect by instructions
  - PC (program counter), condition codes
Instruction Set

Opcodes
- 15 opcodes
- Operate (Logical or Arithmetic) instructions: ADD, AND, NOT
- Data movement instructions: LD, LDI, LDR, LEA, ST, STR, STI
- Control instructions: BR, JSR/JSRR, JMP, RTI, TRAP
- some opcodes set/clear condition codes, based on result:
  - N = negative (< 0), Z = zero, P = positive (> 0)

Data Types
- 16-bit 2’s complement integer

Addressing Modes
- How is the location of an operand specified?
- non-memory addresses: immediate, register
- memory addresses: PC-relative, indirect, base+offset
Operate Instructions

Only three operations: ADD, AND, NOT

Source and destination operands are registers
  – These instructions do not reference memory.
  – ADD and AND can use “immediate” mode,
    where one operand is hard-wired into the instruction.

Will show dataflow diagram with each instruction.
  – illustrates when and where data moves
    to accomplish the desired operation
Note: Src and Dst could be the same register.

Note: works only with registers.
ADD/AND

ADD
0 0 0 1 | Dst | Src1 | 1 | Imm5

AND
0 1 0 1 | Dst | Src1 | 1 | Imm5

Note: Immediate field is sign-extended.
Data Movement Instructions

Load -- read data from memory to register
- LD: PC-relative mode
- LDR: base+offset mode
- LDI: indirect mode

Store -- write data from register to memory
- ST: PC-relative mode
- STR: base+offset mode
- STI: indirect mode

Load effective address -- compute address, save in register
- LEA: immediate mode
  - does not access memory
Addressing Modes

- How memory is addressed.
- Different instructions use different addressing modes.
- Some instructions support more than one addressing mode.
LC-3 Addressing Modes

- **PC-Relative**
  - Address is a displacement from PC

- **Indirect**
  - Use PC-Relative to get address from memory

- **Base plus Offset**
  - Use contents of a register as base address and add offset to find address (most common for load/store architectures)
PC-Relative

The Problem:

We want to specify address directly in the instruction
- But an address is 16 bits, and so is an instruction!
- After subtracting 4 bits for opcode and 3 bits for register, we have only 9 bits available for address.
The Solution:
Use the 9 bits as a *signed offset* from the current PC.

9 bits allows the offset range to be:

\[-256 \leq \text{offset} \leq +255\]

We can now form any address \(X\), such that:

\[(\text{PC} - 256) \leq X \leq (\text{PC} + 255)\]

Remember that the **PC** is incremented as part of the FETCH phase; This is done before the EVALUATE ADDRESS stage.
LD (Load Data)

```
LD 0 0 1 0 Dst PC offset 9
```

Diagram showing the flow of data from PC, through Instruction Reg, Sext, Register File, Memory, MAR, MDR.
Indirect

The Problem:
With PC-relative mode, we can only address data within 256 words of the instruction.

– What about the rest of memory? How do we access it?
Solution #1:

- Read address from memory location, then load/store to that address.

First address is generated from PC and IR (just like PC-relative addressing), then content of that address is used as target for load/store.
LDI

1 0 1 0  Dst  PCoffset9

1. PC
2. Instruction Reg
3. Sext
4. IR[8:0]
5. MAR
6. MDR

Register File

Memory
STI

1011

Src

PC.offset9
Base + Offset

Remember The Problem:
With PC-relative mode, can only address data within 256 words of the instruction.

- What about the rest of memory? How do we access it?
Solution #2:

– Use a register to generate a full 16-bit address.

4 bits for opcode, 3 bits for src/dest register, 3 bits for base register – the remaining 6 bits are used as a signed offset.

– Offset is sign-extended before adding to base register.
Load Effective Address

Computes address like PC-relative (PC plus signed offset) and stores the result into a register.

Note: The *address* is stored in the register, not the contents of the memory location.
LEA (Immediate)

LEA 1110 Dst PCoffset9

Diagram showing the execution of an LEA (Load Effective Address) instruction. The diagram includes:
- PC (Program Counter)
- Sext (Sign Extension)
- IR[8:0] (Instruction Register)
- Instruction Reg
- Register File

The diagram illustrates how the PC offset is calculated and loaded into the destination register (Dst).
Control Instructions

Used to alter the sequence of instructions. This is done by changing the PC.

Conditional Branch

- branch is *taken* if a specified condition is true
  - signed offset is added to PC to yield new PC
- else, the branch is *not taken*
  - PC is not changed, points to the next sequential instruction
Unconditional Branch (or Jump)

– always changes the PC

TRAP

– changes PC to the address of an OS “service routine”
– routine will return control to the next instruction (after TRAP) when finished
Condition Codes

LC-3 has three condition code bits:

N -- negative
Z -- zero
P -- positive (greater than zero)

Set by any instruction that writes a value to a register (ADD, AND, NOT, LD, LDR, LDI, LEA)

Exactly one will be set at all times

-- Based on the last instruction that altered a register
Zero

Negative

Positive
Branch Instruction

- Branch specifies one or more condition codes.
- If the set bit is specified, the branch is taken.
  - PC-relative addressing is used
  - target address is made by adding signed offset (IR[8:0]) to current PC.
If the branch is not taken, the next sequential instruction is executed.

- Note: PC has already been incremented by FETCH stage.
- Note: Target must be within 256 words of BR instruction.
BR (PC-Relative)
Jump is an unconditional branch -- *always* taken.
- Target address is the contents of a register.
- Allows any target address.
Instructions

**TRAP**

<table>
<thead>
<tr>
<th>Vector</th>
<th>Routine</th>
</tr>
</thead>
<tbody>
<tr>
<td>x23</td>
<td>input a character from the keyboard</td>
</tr>
<tr>
<td>x21</td>
<td>output a character to the monitor</td>
</tr>
<tr>
<td>x25</td>
<td>halt the program</td>
</tr>
</tbody>
</table>

Calls a **service routine**, identified by 8-bit “trap vector.”

When routine is done, PC is set to the instruction following TRAP.
Another Example

Count the occurrences of a character in an array

- Program begins at location x3000
- Read character from keyboard
- Load each character from an array
  - An array is a sequence of memory locations
  - Starting address of array is stored in the memory location immediately after the program
- If array character equals input character, increment counter
- End of array is indicated by a special ASCII value: EOT (x04)
- At the end, print the number of characters and halt
  (lets assume there will be less than 10 occurrences of the character)
## Program (page 1 of 2)

<table>
<thead>
<tr>
<th>Address</th>
<th>Instruction Bits</th>
<th>Instruction</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>x3000</td>
<td>0 1 0 1 0 1 0 0 1 0 1 0 1 0 0 0 0 0 0</td>
<td><strong>AND</strong></td>
<td>R2 ← 0 (counter)</td>
</tr>
<tr>
<td>x3001</td>
<td>0 0 1 0 0 1 1 0 0 0 0 1 0 0 0 0 0 0</td>
<td><strong>LD</strong></td>
<td>R3 ← M[x3012] (ptr)</td>
</tr>
<tr>
<td>x3002</td>
<td>1 1 1 1 0 0 0 0 0 0 1 0 0 0 1 1</td>
<td><strong>TRAP</strong></td>
<td>Input to R0 (TRAP x23)</td>
</tr>
<tr>
<td>x3003</td>
<td>0 1 1 0 0 0 1 0 1 1 0 0 0 0 0 0 0 0</td>
<td><strong>LDR</strong></td>
<td>R1 ← M[R3]</td>
</tr>
<tr>
<td>x3004</td>
<td>0 0 0 1 1 0 0 0 0 0 1 1 1 1 1 0 0 0</td>
<td><strong>ADD</strong></td>
<td>R4 ← R1 - 4 (EOT)</td>
</tr>
<tr>
<td>x3005</td>
<td>0 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 0</td>
<td><strong>BRz</strong></td>
<td>If Z, goto x300E</td>
</tr>
<tr>
<td>x3006</td>
<td>1 0 0 1 0 0 1 0 0 1 1 1 1 1 1 1 1 1</td>
<td><strong>NOT</strong></td>
<td>R1 ← NOT R1</td>
</tr>
<tr>
<td>x3007</td>
<td>0 0 0 1 0 0 1 0 0 1 1 0 0 0 0 1</td>
<td><strong>ADD</strong></td>
<td>R1 ← R1 + 1</td>
</tr>
<tr>
<td>x3008</td>
<td>0 0 0 1 0 0 1 0 0 1 0 0 0 0 0 0 0 0</td>
<td><strong>ADD</strong></td>
<td>R1 ← R1 + R0</td>
</tr>
<tr>
<td>x3009</td>
<td>0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 1</td>
<td><strong>BRnp</strong></td>
<td>If N or P, goto x300B</td>
</tr>
<tr>
<td>Address</td>
<td>Instruction Bits</td>
<td>Instruction</td>
<td>Comments</td>
</tr>
<tr>
<td>---------</td>
<td>------------------</td>
<td>-------------</td>
<td>----------</td>
</tr>
<tr>
<td>x300A</td>
<td>0001010010100001</td>
<td>ADD</td>
<td>R2 ← R2 + 1</td>
</tr>
<tr>
<td>x300B</td>
<td>0001101101110001</td>
<td>ADD</td>
<td>R3 ← R3 + 1</td>
</tr>
<tr>
<td>x300C</td>
<td>0110001011100000</td>
<td>LDR</td>
<td>R1 ← M[R3]</td>
</tr>
<tr>
<td>x300D</td>
<td>0000111111110110</td>
<td>BRnzp</td>
<td>Goto x3004</td>
</tr>
<tr>
<td>x300E</td>
<td>0000000000000100</td>
<td>LD</td>
<td>RO ← M[x3013]</td>
</tr>
<tr>
<td>x300F</td>
<td>0001000000000010</td>
<td>ADD</td>
<td>RO ← RO + R2</td>
</tr>
<tr>
<td>x3010</td>
<td>1111000000100001</td>
<td>TRAP</td>
<td>Print RO (TRAP x21)</td>
</tr>
<tr>
<td>x3011</td>
<td>111100000010101</td>
<td>TRAP</td>
<td>HALT (TRAP x25)</td>
</tr>
<tr>
<td>x3012</td>
<td></td>
<td></td>
<td>Starting Address of File</td>
</tr>
<tr>
<td>x3013</td>
<td>0000000000110000</td>
<td>Data</td>
<td>ASCII x30 ('0')</td>
</tr>
</tbody>
</table>

*opcode*
LC-3 Data Path

Filled arrow = info to be processed

Unfilled arrow = control signal.
Data Path Components

Global bus

- special set of wires that carry a 16-bit signal to many components
- inputs to the bus are “tri-state devices,” that only place a signal on the bus when they are enabled
- only one (16-bit) signal should be enabled at any time
  - control unit decides which signal “drives” the bus
- any number of components can read the bus
  - register only captures bus data if it is write-enabled by the control unit

Memory

- Control and data registers for memory and I/O devices
- memory: MAR, MDR (also control signal for read/write)
**ALU**

- Accepts inputs from register file and from sign-extended bits from IR (immediate field).
- Output goes to bus.
  - used by condition code logic, register file, memory

**Register File**

- Two read addresses (SR1, SR2), one write address (DR)
- Input from bus
  - result of ALU operation or memory read
- Two 16-bit outputs
  - used by ALU, PC, memory address
  - data for store instructions passes through ALU
PC and PCMUX

- There are three inputs to PC, controlled by PCMUX
  1. PC+1 – FETCH stage
  2. Address adder – BR, JMP
  3. bus – TRAP (discussed later)

MAR and MARMUX

- There are two inputs to MAR, controlled by MARMUX
  1. Address adder – LD/ST, LDR/STR
  2. Zero-extended IR[7:0] – TRAP (discussed later)
Condition Code Logic
- Looks at value on bus and generates N, Z, P signals
- Registers set only when control unit enables them (LD.CC)
  - only certain instructions set the codes
    (ADD, AND, NOT, LD, LDI, LDR, LEA)

Control Unit – Finite State Machine
- On each machine cycle, changes control signals for next phase of instruction processing
  - who drives the bus? (GatePC, GateALU, ...)
  - which registers are write enabled? (LD.IR, LD.REG, ...)
  - which operation should ALU perform? (ALUK)
  - ...
- Logic includes decoder for opcode, etc.
Summary of ISA

- Instruction Set Architecture
- The ISA provides all the information needed for someone to write a program in machine language (or translate from a high-level language to machine language).
More LC-3 ISA
TRAP Instruction

- Trap vector (trapvect8)
  - identifies which system call to invoke
  - 8-bit index into table of service routine addresses
    - in LC-3, this table is stored in memory at 0x0000 – 0x00FF
    - 8-bit trap vector is zero-extended into 16-bit memory address

- Where to go
  - lookup starting address from table; place in PC

- How to get back
  - saves address of next instruction (current PC) in R7 before changing PC
NOTE: PC has already been incremented during instruction fetch stage.
RET (JMP R7)

How do we transfer control back to instruction following the TRAP?

• Save old PC in R7.
  – JMP R7 gets us back to the user program at the right spot.
  – LC-3 assembly language lets us use RET (return) in place of “JMP R7”.

• Must make sure that service routine does not change R7, or it won’t know where to return.
JSR Instruction

Jumps to a location (like a branch but unconditional), and saves current PC (addr of next instruction) in R7.

- saving the return address is called “linking”
- target address is PC-relative ($PC + \text{Sext}(IR[10:0])$)
- bit 11 specifies addressing mode
  - if =1, PC-relative: target address = $PC + \text{Sext}(IR[10:0])$
  - if =0, register: target address = contents of register IR[8:6]
NOTE: PC has already been incremented during instruction fetch stage.
JSRR Instruction

Just like JSR, except Register addressing mode.
- target address is Base Register
- bit 11 specifies addressing mode

What important feature does JSRR provide that JSR does not?
NOTE: PC has already been incremented during instruction fetch stage.