

CE202 – Computer Architecture

Project Ideas

This is a collection of project ideas on various topics. You may select one of the following topics or come up with your own idea — recent architecture proceedings could be a good place to look. All projects will require location of CURRENT background references. Sources may be found in the text, the library, the WWW, and by chatting with me and other faculty. Several of the problems in the text could be expanded into projects. I find that IEEE Micro frequently has excellent overview articles in computer architecture, with citations to valuable source material.

The short project proposal should include a clear statement of the problem, the approach you will use, approaches others have used, references, and why the problem is interesting, and a schedule of the work you will do and tools you will use.

The progress reports should include, in addition to your progress in relation to the project proposal, a completed background literature review. I am tentatively planning to have a peer-review component to the progress reports to help cope with the large class size.

Projects can be experimental, theoretical, or research review-oriented. An experimental project should follow standard scientific method of having some idea that you wish to test, and a means of testing it. A theoretical paper could perform a mathematical analysis of some system coupled with an evaluation of your results. A research review report will include a thorough review of a topic drawing from many technical articles. Reports in the research review category will be held to a higher standard than those that include theoretical or experimental results as well.

All reports must place themselves in the greater context of the field. All reports that use computers (for example, to simulate something) must include the performance information about the simulations as well as the results.

The final report should be suitable for submission to a conference. If you are including code or data, be sure to place it in an appendix rather than in the paper.

Joint projects, if approved, require exceedingly clear and specific divisions of work in the short proposal, progress report, and the final report.

The initial project proposal must include: 1. the title of the project; 2. A short description of the project; 3. your expected results (what will you prove or disprove? why is it interesting?) 4. A list of references for the project; 5. a thorough description of the division of labor if it is a joint proposal; and 6. a thorough description of any previous or concurrent work that relates to this project. Please number these items. (And don't forget 0. Your name).

Parallel Processing Kestrel is a linear array of 8-bit processing elements. Several applications have been studied on Kestrel (its target sequence analysis, as well as FFT, DCT, and neural networks), as well as multiplicative division algorithms using its 8-bit multiplier. Some of the possible projects here would include:

- Studying one or more other math functions (e.g., sine, log, square root, ...) for efficient implementation.
- Implementing other applications (or taking one of the existing ones, such as neural networks, refining it, and using it for some real studies).
- Analyzing board and chip tradeoffs to discover what the good design points are for massively parallel, fine grain parallel processor.

- Deciding how we can build and MSIMD machine; a machine composed of several SIMD broadcast instruction machines with independent controllers connected by some sort of network.

Other research projects There are plenty of other research projects in computer architecture and computer system design. You may be able to find a topic of interest to another faculty member that you can turn into an MS or Ph.D. thesis.

New architectures There are regularly articles on the implications of new technologies on architecture. Topics include:

- Simultaneous multithreading. Keeping several independent jobs active in the superscalar pipeline to reduce stalls by providing more independent instruction streams. This project could be a hardware evaluation and design of what resources must be replicated, coupled with some realistic trace analysis.
- Simultaneous multithreaded vector processing. A coupling of multithreaded with vector instructions (single instructions that process many data items).
- SIMD Extensions. E.g., things like MMX. Evaluate how such can affect performance or do an extensive survey of different approaches to this idea.

Low-power architectures . Wireless, handheld-held, and sensor-net systems have particular need for low-powered architectures. What techniques are used in creating these designs, and what is the impact on performance?

IEEE TC The following articles from IEEE Transactions on Computers have caught my eye for potential projects in extending, reproducing, or evaluating results:

- “A dynamically tunable memory hierarchy,” Balasubramonian et al, 52(10):1243.
- “Special section on cryptographic hardware and embedded systems,” Koc and Paar, ed, 52 (4). Consider using Kestrel or enhancing the simple scaler simulator to include instructions that will assist in cryptographic applications, and analyze performance.
- “Measuring the performance of multimedia instruction sets,” Slingerland and Smith, 51(11): 1317. Extend the methodology to PIV/SSE.
- “Hybrid load-value predictors”, Burtscher and Zorn, 51 (7): 759. We have talked about branch prediction, how about load prediction? Analyze how load value prediction can help (or hurt) performance.
- “Reducing memory latency for a read-after-read memory dependents prediction,” Moshovos and Sohi, 51 (3): 313. Does it really help?
- “Special Section on High Performance Memory Systems”, Hadimioglu, Kaeli, and Lombardi, eds. 50(11), November 2001.
- “Dynamic multiple parity (DMP) disk array for serial transaction processing”, Yeung and Yum, 50(9):949, September 2001.
- “Lookahead scheduling requests for multisource page caching,” Kiniwa, Hamada, Mizoguchi, 50(9):972, September 2001.
- “Inherently lower-power high-performance superscalar architectures”, Zyuban and Kogge, 50(3):268, March 2001.

- “Memory hierarchy considerations for cost-effective cluster computing”, 49(9), September 2000.
- “Exploiting the role as a main geometry processing with general-purpose processors and floating-point SIMD constructions”, 49(9), September 2000.

IEEE TPDS The following articles from IEEE Transactions on Parallel and Distributed Systems have caught my eye for potential projects in extending, reproducing, or evaluating results:

- “RAPID-CACHE — A reliable and inexpensive write cache for higher performance storage systems,” 13(3):290, March 2002.
- “Compiler-assisted multiple instruction word retry for VLIW architectures,” 12(12):1293, December 2001.

More on Multithreading The September 1999 issue of IEEE Transactions on Computers has a special section on multithreading. Try simulating one of the proposed architectures (possibly with modification) to confirm or refute their results.

Hot Chips The March/April issues of MICRO include articles from the Hot Chips conference. These can provide pointers to other references or ideas, such as analyzing whether or not a specific architectural feature seems worthwhile.

Workload The February 2003 issue of Computer has many articles on different types of workload. Try to find some of these workloads and analyze their characteristics on some machines and simulators that you have access to.

Pipeline Analysis SimpleScalar is a pipeline simulator available in `/cse/classes/cmpe202/SimpleScalar`. Modify `sim-outoforder` to mirror the P4 architecture (or another) pipeline, and see how things work, and compare to the original simulator.

Textbook The textbook has a number of project-level problems.