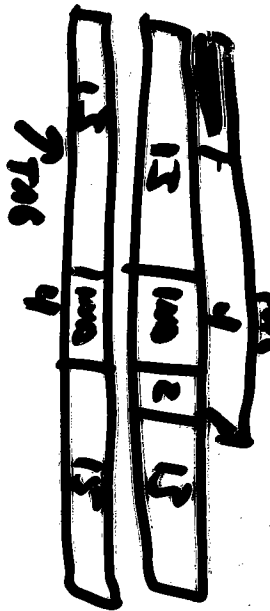


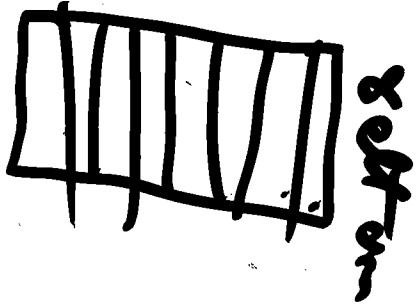
84  
32 041



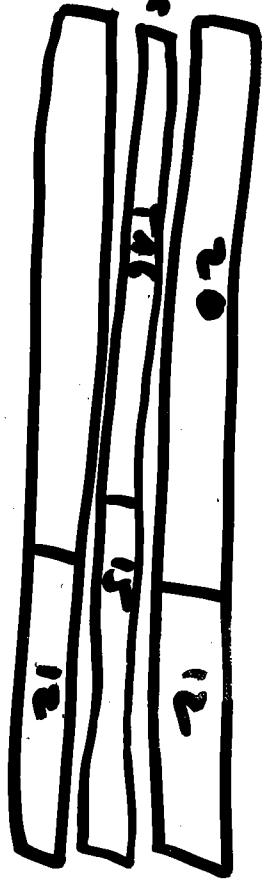
100 120  
any 120, 2-way  
32-bit odd



04



VA 32  
Card mdr  
PA 32



TLG

Hit--

DM

2-w

4-w

8-w

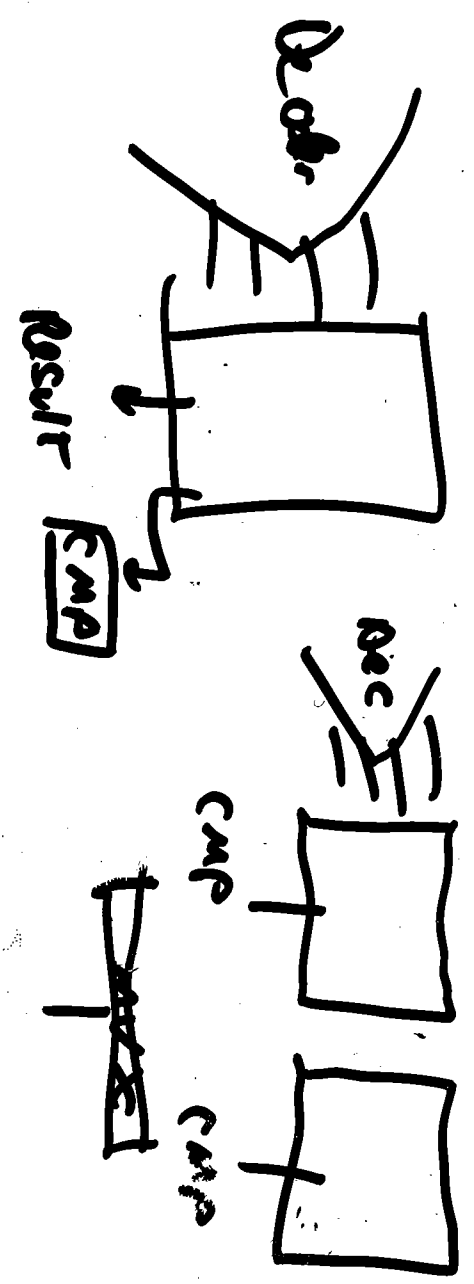
Fully Assoc

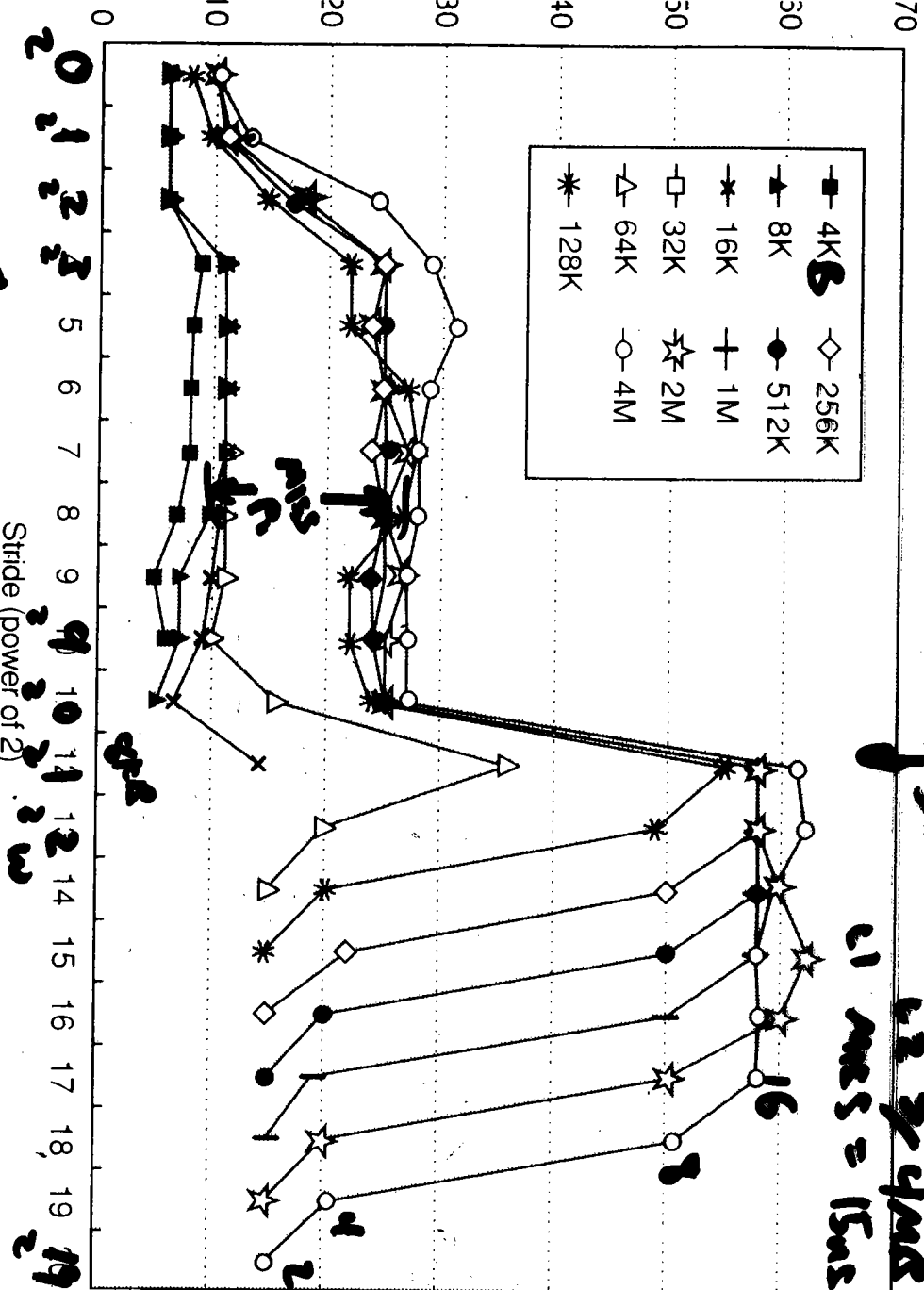
HIT 4+

si

Time & Space

Room for  
comp.  
Space--





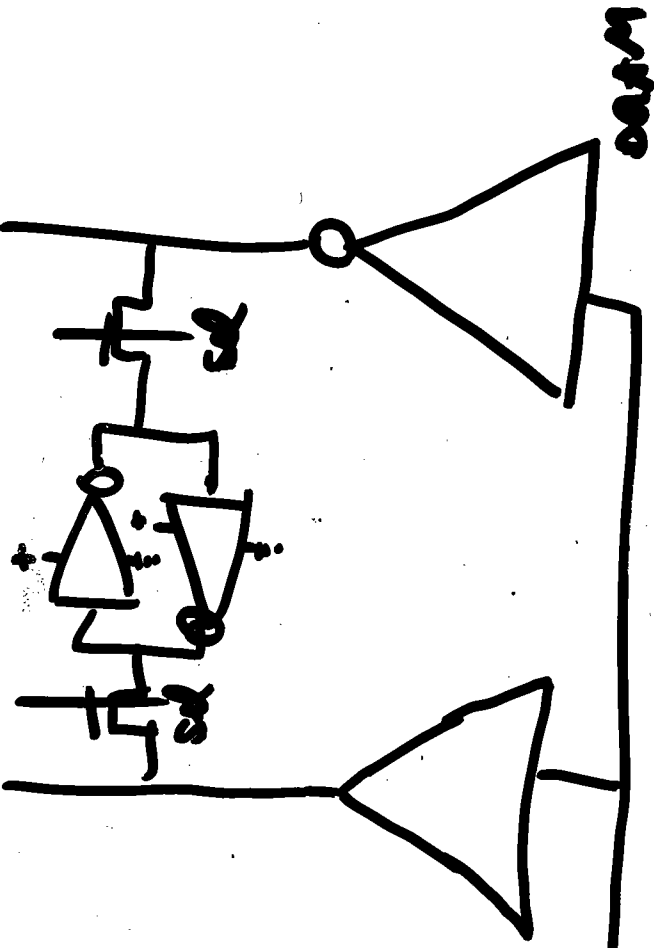
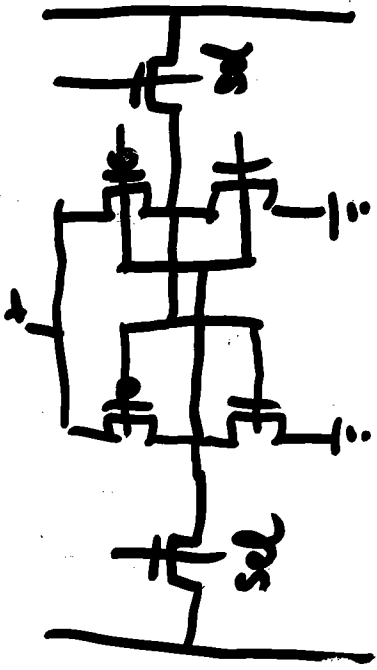
miss  
L2 = 25ns  
L2 = 37ns  
L1 miss = 15ns

Block = 8w 10ns for L2 L2 = 64KB

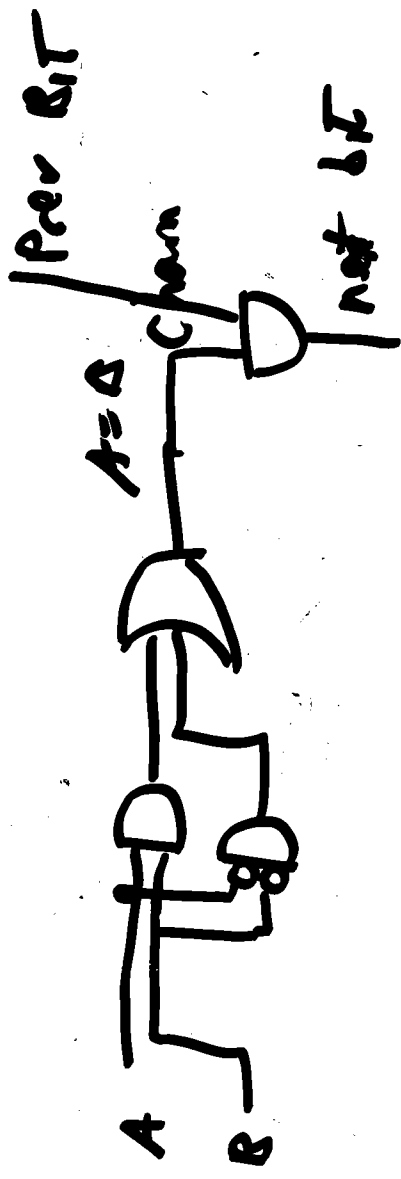
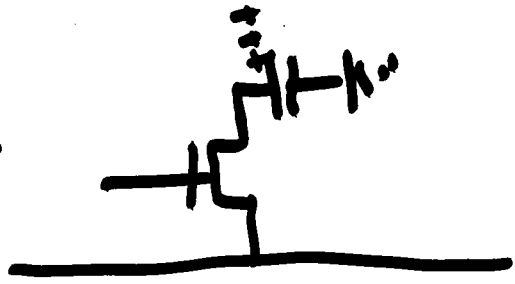
Results of running program in Exercise 5.2 on a Sun Blade 1000.

L1B ~ 8 entries based on Δ for data

System for this computer is composed of a split L1 cache that is direct mapped and 2-way set associative. Both the I-cache and D-cache are direct mapped and 2-way set associative. The I-cache has a 2% miss rate and 32-byte blocks, and the D-cache has a 5% miss rate and 16-byte blocks. There is a write-back cache that eliminates stalls for 95% of all writes.



value to write



COMPARATOR =  $\sim 2-3x$  SAMM cell