~~0.004~~ 0.004 of instr cause 8-cycle stall

lose 3 instr/clock.

~~Cost is 24 instructions~~

or

2 slots/instr.

except IF reques $24 \cdot 0.004 = .096 =$ 0.1

extra slots/inst

2.1 slots/instr. $\frac{6}{2.1} = IPC$

IF ISI IS2 IS3

CONTROL - 14%, stalls/instr = 0.16

$$\frac{\text{clocks}}{\text{Instr}} = 1.16 \qquad \text{control}$$

$$\frac{\text{slots}}{\text{Instr}} = 2.0 \qquad \text{OTB - (50\% of peak)}$$

$IR_{peak} = 6$

$$IPC_{eff} = IPC_{peak} \cdot \text{Eff}$$

$$\frac{\text{slots}}{\text{clock}} = 6$$

$$\frac{\text{slots}}{\text{Branch}} = 1 + 6 \cdot .16 = 1.96$$

$$\text{Ave slots/Instr} = (0.86)(2) + (0.14)(1.96) \simeq 2$$

$$IPC_{real} = \frac{IPC_{peak}}{(\text{slots/Instr})_{ave}} = 3$$

(f) (10 points) If a cache miss happens, an additional 8 cycles are required to access the on-chip 256K L2 cache. The L1 caches are 16K. If L2 fits all memory necessary for a program, and the instruction cache miss rate is 0.4%, and the data cache miss rate is 6% (estimated from table 5.7 for a 16K cache), what is IPC considering cache misses? Assume that instruction cache misses fully stall the pipeline, but that there are sufficient reservation stations so that other instructions may execute during a data cache miss.

(g) (10 points) Consider the merging of DET and WB. What would the implications of this be? What issues would come up in deciding whether or not to merge the two stages?

(h) (10 points) Why is instruction issue rate insufficient for comparing different processors?

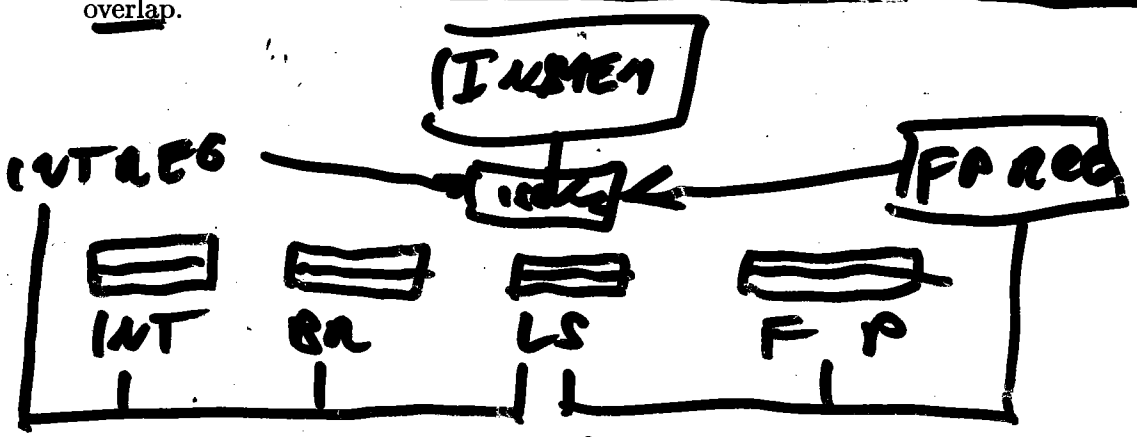
(i) (Extra credit) Design a VLSI layout for this architecture.

2. (10 points) Dynamic instruction scheduling

Consider a Tomosulo pipeline (similar to PowerPC 620 in text) with stages IF, ID, IS (the process of moving instructions to reservation stations), EX (1 cycle integer, 2-cycle LSU, 3-cycle FP mult or add), and WB (commit). There is one integer unit with two reservation stations (I1, I2), 1 FP unit with two reservation stations (F1, F2), 1 Load/Store unit with two reservation stations (LS1, LS2), and one Branch unit with 2 reservation stations (B1, B2) that takes 1 cycle.

Indicate the clock cycle for each of the following instructions would be in the various stages. Assume 1 instruction issue per cycle and serparate FP and integer result busses. Assume that

In the RS# column indicate the reservation station slot (e.g., F1, I2, B1) that was used. For an instruction already in a reservation station, EX1 can commence during the same cycle as the common data bus write in WB. EX2 and EX3 are not used for all instructions — leave blank for those that do not need them. A new instruction can be loaded into a reservation station when the old one is in WB — WB and IS can overlap.



I1/2 SCALAR
F1/2
L1/2
Q1/2

B
INT LSU FP
1 1 1

	IF	ID	IS	EX1	EX2	EX3	WB	RS #
foo: LD F2, 0(R1)	1	2	3	4	5		6	L1
MULTD F5, F2, F2	2	3	4	6	7	8	9	F1
MULTD F4, F5, F0	3	4	5	9	10	11	12	F2
LD F6, 0(R2)	4	5	6	7	8		10	L1
ADDD F6, F4, F6	5	6	9	12	13	14	15	F1
SD 0(R2), F6	6	7	10	15	16			L2
ADDI R1, R1, #8	7	8	11	12			13	I2
ADDI R2, R2, #8	8	9	12	13			14	I2
SGTI R3, R1, done	9	10	13	14			15	I2
BNEQZ R3, foo	10	11	14	15				

Spare diagram:

	IF	ID	IS	EX1	EX2	EX3	WB	RS #
foo: LD F2, 0(R1)								
MULTD F5, F2, F2								
MULTD F4, F5, F0								
LD F6, 0(R2)								
ADDD F6, F4, F6								
SD 0(R2), F6								
ADDI R1, R1, #8								
ADDI R2, R2, #8								
SGTI R3, R1, done								
BNEQZ R3, foo								

3. (10 points) How can performance be improved in problem 2?