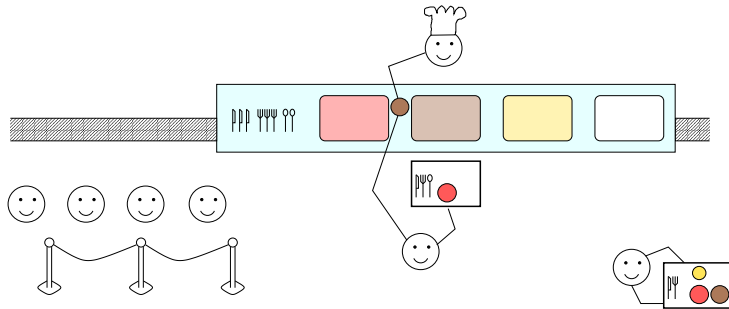


Multicycle restaurant

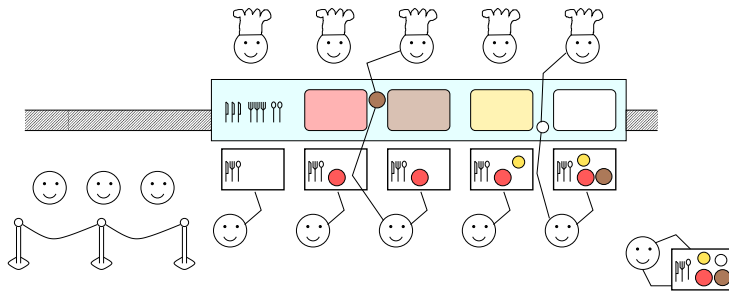


CMPE011 Fall 2003 Pipelined CPU

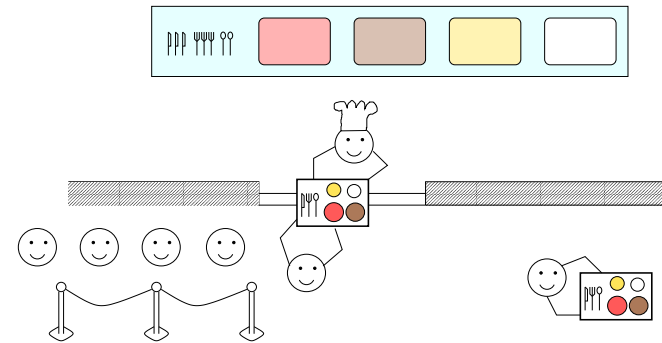
- Pipeline principles
- Pipelinedatapath
- Pipelined control

Textbook: 6.1 to 6.3

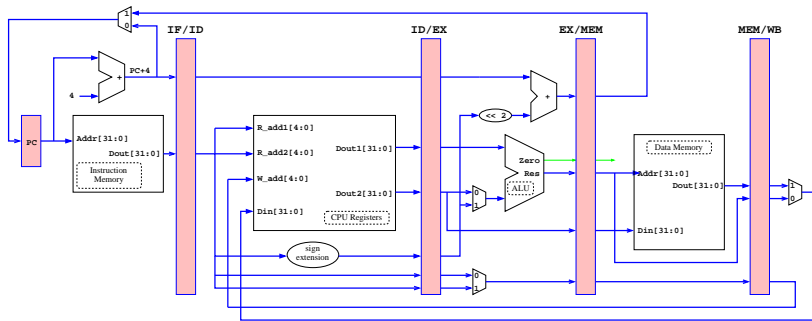
Pipelined restaurant



Single-cycle restaurant



Pipelined datapath



Pipelined datapath

What is a “pipeline”?

- just like in the multicycle datapath, there are *stages*
- in a pipelined architecture, however, all stages operate concurrently
- a new instruction begins execution at every clock cycle

Pipeline characteristics

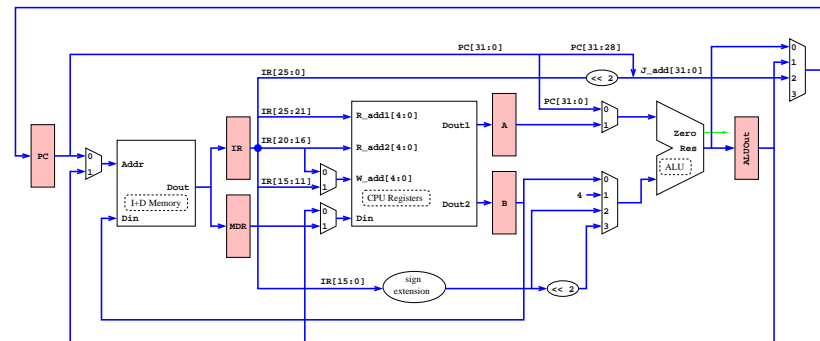
number of stages: five in the classical pipeline

(IF, ID, EX, MEM, WB — just like in the multicycle CPU)

T_{ck} limitation: now the constraint is the longest worst-case path among all the stages

resources: to perform some operations concurrently, we need to duplicate some resources (like in the single-cycle implementation)

Our multicycle datapath



Pipeline performance

speedup: ideal speedup = # of pipeline stages
(only if the stages are perfectly balanced)

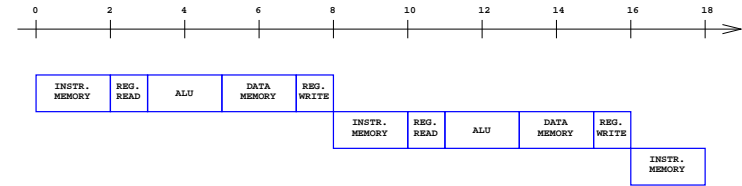
CPI: ?

throughput: we approach the ideal speedup only when considering the execution of many instructions

latency time: the execution time of a single instruction



Single-cycle vs. pipeline execution

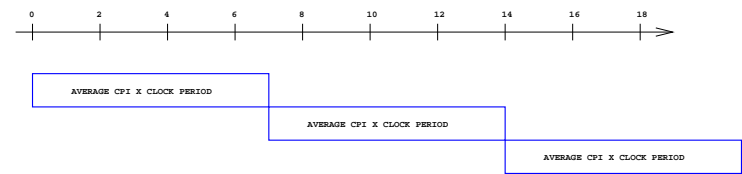


MIPS instruction set architecture and pipelining

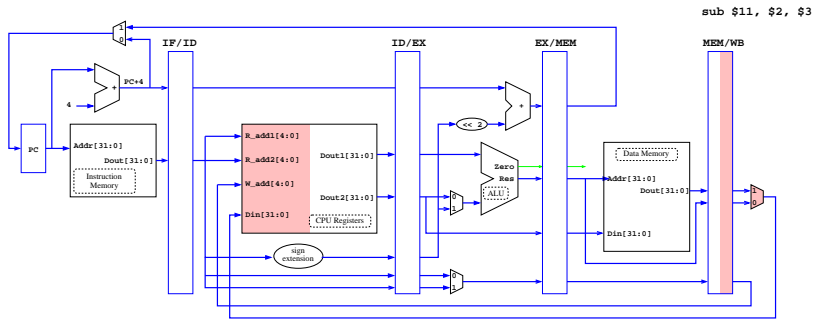
- all instructions are the same length
- few instruction formats (and very similar)
- memory accesses only in load/store instructions



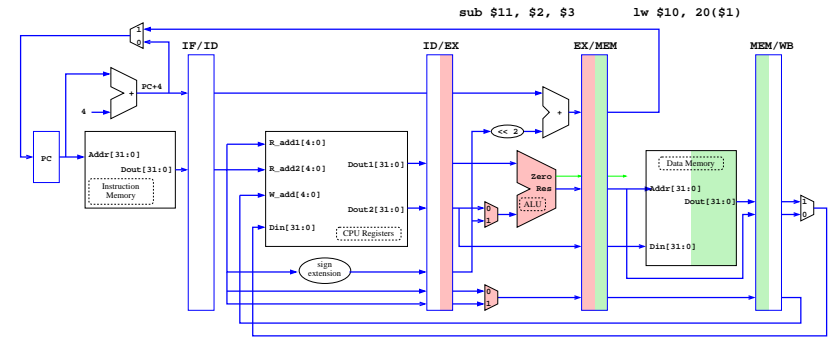
Multicycle vs. pipeline execution



A walk through the pipeline: clock cycle 6

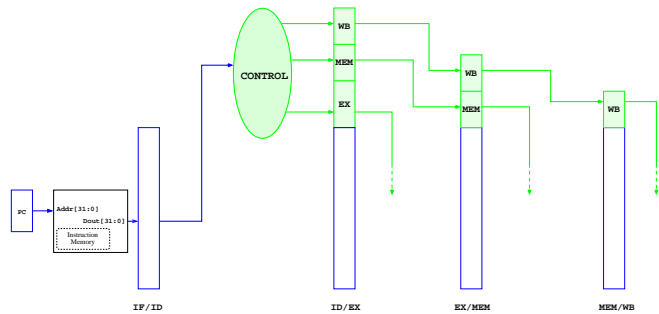


A walk through the pipeline: clock cycle 4

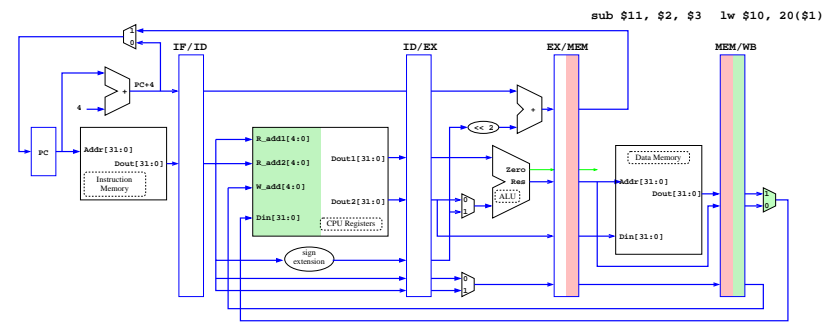


Pipelined control

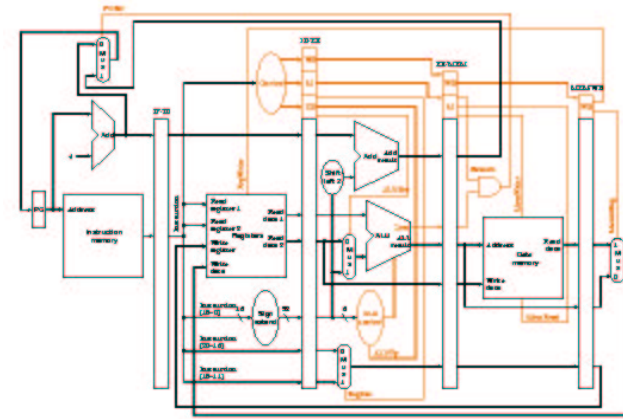
- pipelining the datapath leaves the meaning of control lines unchanged
- control signals are pipelined too (grouped by stage)
- the control unit is combinatorial again



A walk through the pipeline: clock cycle 5



Pipelined control: complete schematic



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Recommended exercises

Ex. 6.5, 6.7, 6.9, 6.10

